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COST OPTIMIZATION IN LOW
VOLUME VLSI CIRCUITS

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Definition of Symbols

<u>Symbol</u>	<u>Definition</u>
A	active die area
A_1	area of a single memory storage cell
A_d	MOS memory chip die area
A_G	average gate area
A_i	active die area for i th masking level
A_{max}	maximum chip area by computer generated layout
A_{min}	theoretical minimum chip area
B	proportion of module failures which are not repairable
B_1	area required for interconnecting gates, peripheral area and bond pad area
BP	bond pad area
β	chip area optimization efficiency constant
β_0	chip area optimization efficiency constant independent of NG
D_i	defects/unit area produced by the i th masking level
D_n	average defect density over all n masking levels
$\$A$	initial acquisition cost or initial cost of manufacture of the system per system
$\$AC$	assembly cost per IC successfully completing manufacture
$\$CA$	total cost, excluding IC cost, of all system components and all assembly, design, fabrication and testing cost
$\$CAD$	layout cost per unit time
$\$CB$	cost of spare connectors and boards

\$CE	burdened circuit designer labor cost
\$CR	circuit design cost
\$D	die cost
\$DM	LSI device manufacturing cost
\$(d/l)	design/layout cost
\$F	total fab cost of all wafers produced
\$L	layout cost
\$ML	cost per unit time for manual layout optimization
\$R	system repair or module replacement cost
\$RE	reticle fab cost
\$RPL	cost to replace a module
\$RPR	cost to repair a module
\$S	cost per system of spare parts
\$T	total cost of a single electronic system (direct life cycle cost)
\$TC	total test cost per successful IC
\$W	cost per wafer out of fab
f	number of hand optimized critical mask levels
K_A	defined as A/Ad
K_C	bond pads per chip
K_p	average number of pins per gate
K_1	experience constant defined by eq. (37)
K_3	experience constant defined by eq. (39)
K_{21}	experience constant defined by eq. (38)
K_{22}	experience constant defined by eq. (38)
K_{23}	experience constant defined by eq. (38)

λ_g	IC failure rate per gate-hour
λ_i	failure rate for ith IC
λ_s	system failure rate
MU	mark up by IC vendor to cover profit and cost of sales
M_r	number of reticles
(MTBF) _i	mean time before failure of ith IC
n	number of defect producing, yield limiting photo masking operations
N	total number of gates per system
NA	number of applications of a chip per system
N_c	IC's per module
ND	total number of die on a wafer
NES	total number of electronic systems for the total program
NESS	total number of electronic subsystems or modules per program
(NG) _i	total number of gates per ith IC
NI	total number of IC's per system
N_m	total number of successful IC's of a certain type manufactured
N_0	number of bits in memory
NSCB	number of spare connectors and boards for repairable modules
NSM	number of spare modules
R_1	coefficient to determine area contribution by row and column decode and sense circuitry
R_2	coefficient to determine peripheral area contribution
t	time
t _c	circuit design time
t _{cad}	CAD layout time

T_L	electronic system total operational life
t_{ML}	manual layout time
Y_A	assembly yield
Y_D	yield of IC die on a silicon wafer at probe test
Y_F	wafer fab yield
Y_T	total IC yield
Y_{FT}	final test yield

CONTRACTOR REPORT

FINAL REPORT

Cost Optimization in Low Volume VLSI Circuits

Summary

In this report, the relationship of integrated circuit cost to electronic system cost is developed using models for integrated circuit cost which are based on design/fabrication approach. Emphasis is on understanding the relationship between cost and volume for custom circuits suitable for NASA applications. In this regard, reliability is a major consideration in the models developed. Results are given for several typical IC designs using off-the-shelf, full-custom, and semi-custom IC's with single and double-level metallization.

I. INTRODUCTION

The purpose of this report is to examine the relationship of integrated circuit cost to electronic system cost, to develop models to predict integrated circuit cost and thus resulting electronic system cost and to examine the various parameters which affect integrated circuit cost. The emphasis of this report is on the development of an understanding of the cost of VLSI (very large scale integrated circuits) and in particular the effects of low volume and large die area on cost.

A simple macroscopic cost model of an electronic system is developed in which it is assumed that the system under consideration is to be partitioned into subsystems consisting of integrated circuit chips. The aim is to examine the resulting system cost due to variation in the parameters which affect LSI die cost. Since emphasis is to be placed on the factors which affect die cost, the systems calculations and modeling are kept to a minimum.

A macroscopic cost model for an integrated circuit is developed which is intended to be sufficiently general to include all aspects of IC manufacture such as choice of device type, choice of process technology, choice of packaging and effects of both quantity manufactured and die area. The report includes discussions of present process and fabrication alternatives and their potential impact on chip cost.

Although cost models developed are general in nature, the purpose is to examine the costs of low volume, custom integrated circuits suitable

for NASA applications. In this regard reliability will be a major consideration in the choice of design/process alternatives and as much as possible the impact of reliability will be included in the modeling.

It is not the purpose of this phase of the effort to treat the subject of integrated electronics cost in detail but to establish the initial framework from which further, more detailed, work can proceed. Also, it is not the purpose of the report to treat the cost of an electronic system in detail but to establish the trends and guidelines necessary for further work. Thus, detailed analysis of system costs are not included herein.

The trend in the design of electronic systems is clearly toward combining more and more electronic functions into smaller and smaller volumes. The gains in reliability, weight reduction, speed, etc. are well known. The rate at which large electronic systems have been "integrated" and the total number of components reduced has been equally offset by increases in system complexity. The continued development of sophisticated electronics systems requires the continued use of integration of more and more electronic functions on single integrated circuit chips. We have moved rapidly in a period of twenty years from discrete solid state devices to Very Large Scale Integrated circuits (VLSI) containing as many as 75,000 transistors today as shown in Figure 1 [1].

Most applications of integrated electronics during the period 1960-1970 were evolutionary in nature, leading to essentially the same type of equipment but with improved performance, and/or lower cost and smaller physical size. An example was the introduction of minicomputers in the late 1960's, which had essentially the same computing power as some of the

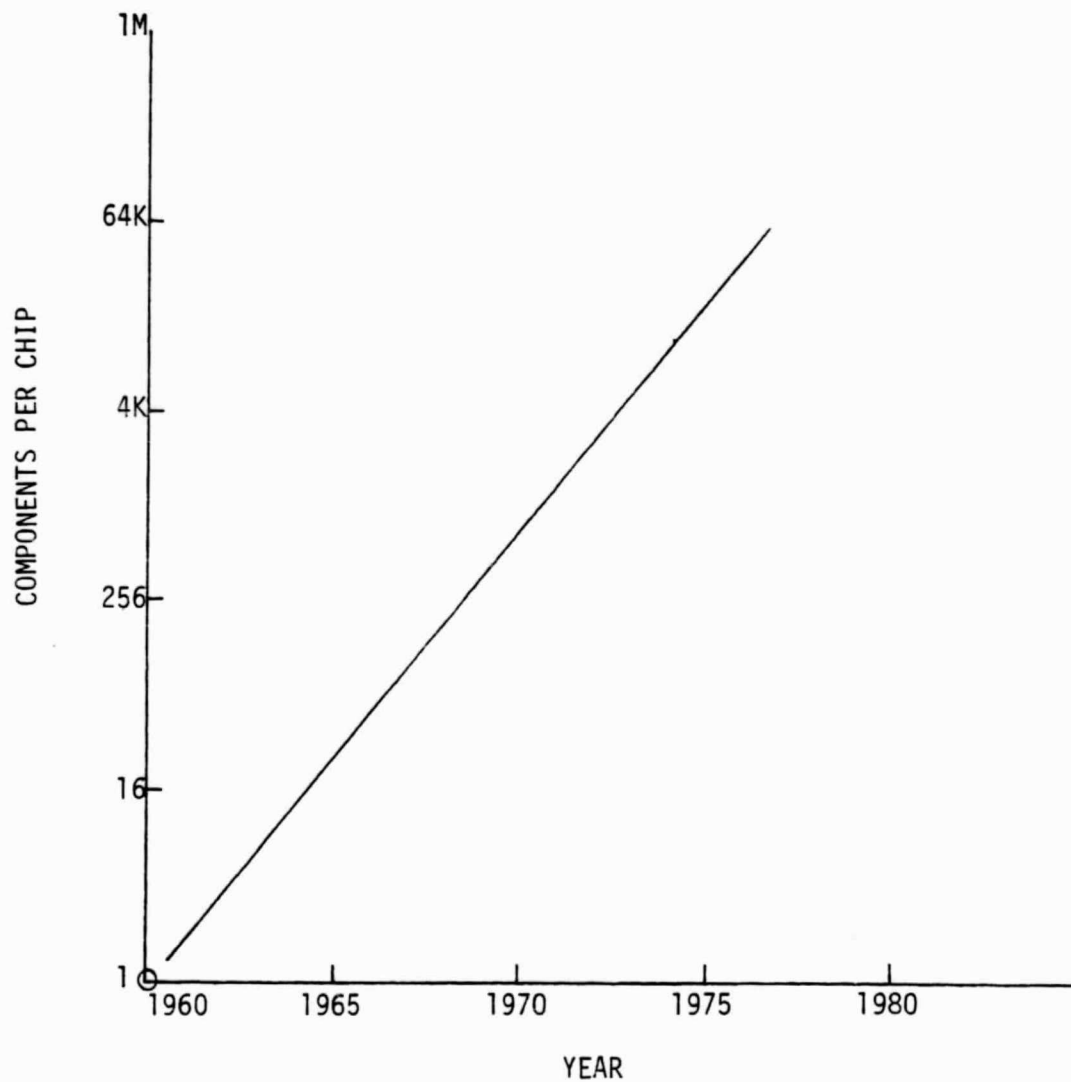


Fig. 1. Approximate component count for complex integrated circuits as a function of year of introduction.

larger computers of earlier years. Similar changes were taking place in the factory; for example, in control equipment for machine tools, with each succeeding generation having performance advantages relative to its predecessor. The first such equipment appeared in 1955, using electron tubes and electromechanical components; five years later discrete transistors were employed; and the third generation of equipment, introduced in 1967, used integrated circuits of relatively small complexity, termed SSI (Small-Scale Integration).

However, as the degree of integration continued to increase into what came to be known as LSI (Large-Scale Integration), some evolutionary developments began to occur. It became possible to fabricate complete system functions in one or a series of LSI chips, making possible a product that simply was not feasible if constructed by other approaches.

Perhaps the most widely known example of LSI leading to an entire new class of product is the personal, hand-held calculator. The development of this product, which has continued beyond the 1960's and into the present, has been another, somewhat different, example of the evolution brought about by LSI is in the area of memories for digital computers. In this case, perfectly satisfactory memory components (magnetic cores) have been used in digital computers since about 1953, whereas the first memory components fabricated in a semiconductor chip were more expensive than cores. However, following the patterns indicated in Fig. 1, the complexity of memory chips increased steadily from the 256 bits available in 1970 to the 64K bits available in 1979.

The cost of semiconductor memory has at the same time decreased below that of magnetic memory components by the use of high technology and high volume production as shown in Fig. 2.

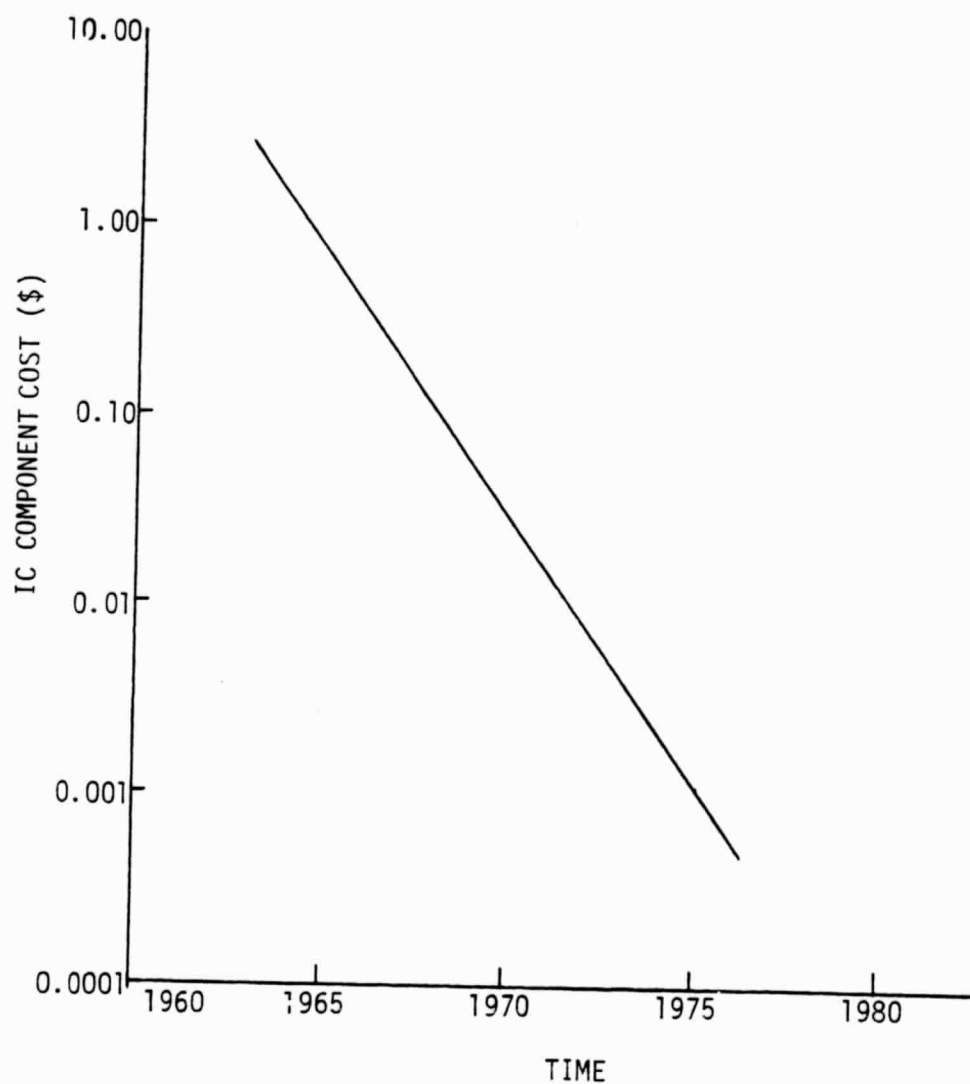


Fig. 2. Average price per component in an integrated circuit as a function of year of introduction.

Although the examples cited above were very successful, practical applications of LSI technology, they happened to have a certain unique property in that they were needed in large volumes. Earliest SSI digital integrated circuits and their somewhat more complex successors, termed MSI (Medium-Scale Integration) circuits were basic building blocks that could be used in a wide variety of applications. However, as the degree of potential integration increased into LSI and VLSI, the resulting, complex circuits tended to be very specialized, each with only one or a few possible applications. If the specialized application happens to involve a large volume of usage, as is the case with the personal calculator and with the semiconductor memory chip, then fixed costs such as those of design and of developing test programs can be amortized over a large number of chips, and the chip can be produced in large volume, which is a requisite for lowest cost. On the other hand, in applications that do not require a large volume of usage, costs are substantially larger.

Electronic systems for NASA will use a mix of high volume and low volume integrated circuits. The choice of the optimum mix for each particular system is a complex problem with parameters which change rapidly. It is therefore imperative to have a practical model of system cost to assist in defining and designing minimum cost systems. The cost of high volume off-the-shelf parts is available from manufacturers price lists. The cost of integrating these standard parts into the system is not included in depth in this work. The designer should plan various levels of usage of off-the-shelf parts and determine their purchase costs. Then the complementary levels of remaining electronics should be defined as "systems"

to the following cost model. Within each level plan, parameters which are a function of partitioning and technology can be exercised.

At this point we have several system approaches defined (level plans plus their implementation sub-plans) with the parts costs for each approach determined including chip design and test costs. The designer must now estimate the cost of the electronic design (including microprogramming if applicable) and overall testing for each approach. Finally, the cost of packaging the above parts must be determined through the use of a packaging cost model being developed by Hughes Aircraft Company under NAS8-32607. Simple addition will provide the cost of each approach from which design decisions can be made.

II. MACROSCOPIC MODEL OF ELECTRONIC SYSTEM COST

A. Basic Assumptions

In this analysis we assume that we have an electronic system which is partitioned in some way into LSI chips. The system is assumed to be composed of sub assemblies which contain the LSI in some degree (SSI, MSI, LSI, etc.). The cost of the entire system is then related to sub assembly cost. The number of sub assemblies is a variable depending on the level of integration.

B. System Cost Factors

Additional understanding of the impact of VLSI on electronic systems is realized through definition of the various cost factors at the system level. These cost factors are simply the sum total of the various costs that accrue during the creating and manufacturing of an electronic system. These factors are:

1. Component cost. This cost includes electronic elements such as resistors, diodes, TTL, LSI Chips, etc. Mechanical components are also part of these expenditures.
2. Tooling cost. This item encompasses engineering labor costs and materials expenses such as printed circuit board layout and procurement. Basically it is a one-time engineering charge.
3. Assembly cost. This expense is incurred in the physical structuring of the system.
4. System testing. Included in this item are debugging of system operation and establishment of system reliability.

5. System repair and maintenance.

6. Inventory. This expense arises from the requirement for stocking component spare parts for the system.

Each of the above six factors must be considered for any electrical system that is to be produced. The relative importance of each of the system cost factors depends, of course, upon the particular system to be manufactured and the total number of systems to be built.

C. Mathematical Model

In this section a mathematical model is presented for the cost of an electronic system composed of assemblies of IC's grouped on subsystems or modules such as pc boards with connectors. We make the following definitions:

N = total number of gates per system

$(NG)_i$ = total number of gates per i th IC where $1 \leq i \leq NI$

NES = total number of electronic systems for the total program

$NESS$ = total number of electronic subsystems or modules per program

NI = total number of IC's per system

To be general we assume subsystem types are not identical and label them as subsystem type 1, 2... i ; Thus we have

$(NESS)_i$ = total number of type i electronic subsystems or modules per program. By definition

$$NESS = \sum_{i=1}^j (NESS)_i \text{ where there are } j \text{ type subsystems or modules (1)}$$

The total cost of a single electronic system (the direct life cycle cost) can be expressed as:

$$\$T = \$A + \$S + \$R \quad (2)$$

where

\$A\$ = initial aquisition cost or initial cost of manufacture of the system per system

\$S\$ = cost per system of spare parts

\$R\$ = system repair or module replacement cost

\$A\$, the initial cost of manufacture, is determined by cost factors 1-4, \$S\$, the cost of spare parts is determined by cost factor 1 and 6 and \$R\$, the system repair cost, is determined by cost factors 4 and 5.

Let the failure rate associated with the i th IC be λ_i . Then we define:

$$(MTBF)_i = \frac{1}{\lambda_i} \quad (3)$$

$(MTBF)_i$ is the mean time before failure associated with the i th IC.

If a system is composed of NI IC's, the corresponding system MTBF becomes:

$$\text{System MTBF} = \frac{1}{\sum_{j=1}^{NI} \lambda_j} = \frac{1}{\lambda_s} \quad (4)$$

if we assume all component associated failures are independent, that the system does not have fault-tolerant design to circumvent the effects of an IC associated failure and that each λ_j includes a share of the interconnection scheme. Alternative equations can be developed to describe the MTBF of systems with fault-tolerant design. [8] These will not be presented in this report. IC associated failure rates are dependent on the number of pads of an LSI chip because most IC failures (non-infant) are associated with the mechanical portions of the device - pins, tabs, connectors, etc. However, since the number of pads does not increase as rapidly as the gate count, the move

from S.S.I. to V.L.S.I. can result in an improvement in reliability by the resulting net reduction in apparent failure rate/gate. This is shown in Figure 3. Curve (1) demonstrates that the failure rate of a chip is proportional to the number of pads which is in turn proportional to the \sqrt{NG} .

Thus,

$$\lambda_g \sim \frac{1}{\sqrt{NG}}$$

Also, in Figure 3 is indicated another factor, curve (2) which shows the effect of pushing the degree of integration beyond the capability of the technology. This is related to LSI process technology and design rules. [9] Another estimate of the apparent individual IC failure rate, λ_i , is given by $2.5 \times 10^{-6} \log(NG)_i$ if the failure rate of the board and its connector is included. [2] This simply shows that system failure is mainly a function of the number of IC packages.

The number of spare modules which must be available for replacement (NSM), is determined by the proportion of module failures which are not repairable, B. If the total operational life of the electronic system is TL, then

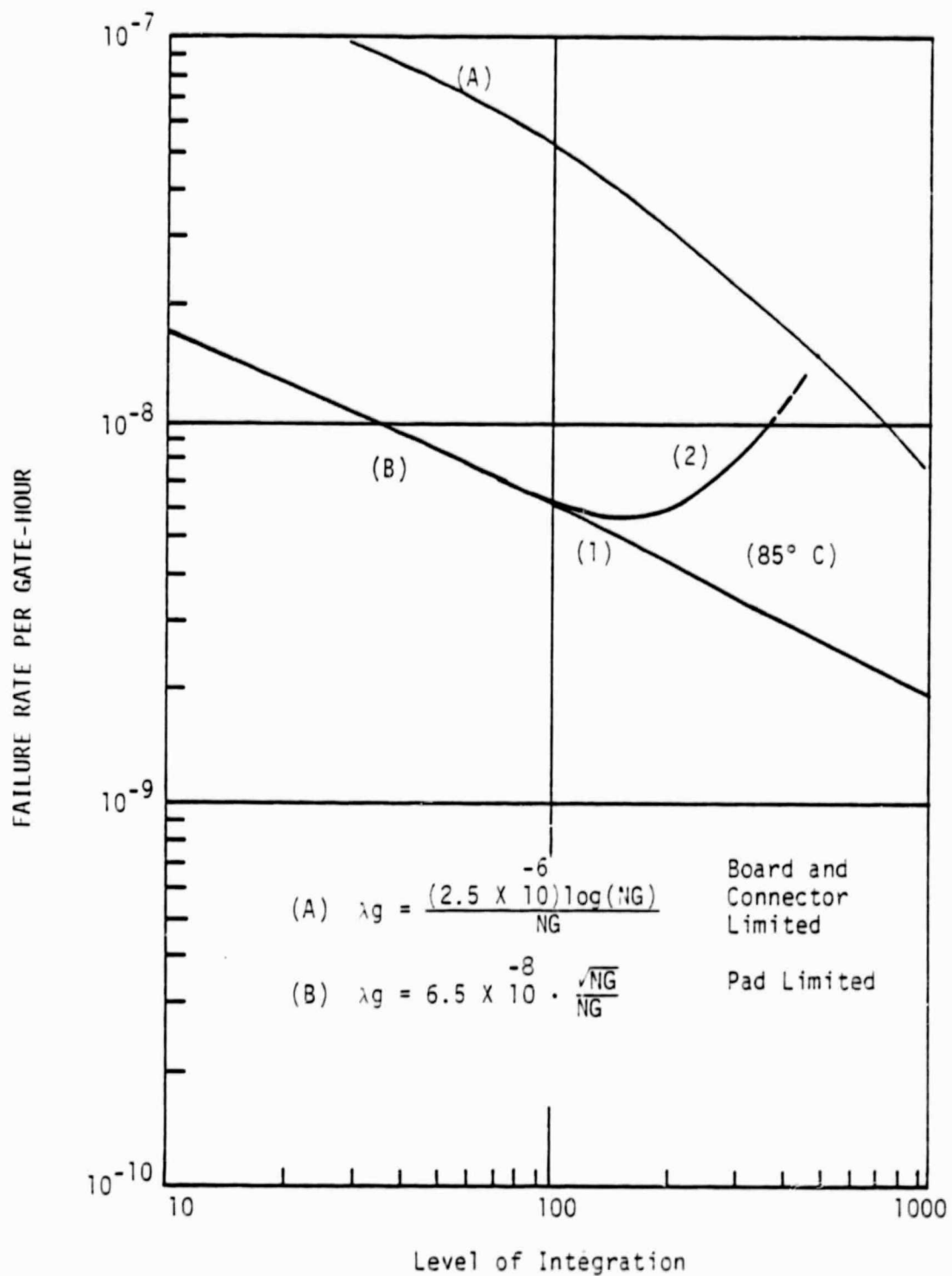
$$NSM = B \cdot \lambda_s \cdot TL \cdot NES \quad (5)$$

and the number of spare connectors and boards for repairable modules is

$$NSCB = (1-B) \cdot \lambda_s \cdot TL \cdot NES \quad (6)$$

The total cost of spare parts (\$S·NES) is then

$$\$S \cdot NES = \$A \cdot NSM \cdot \frac{NES}{NESS} + \$CB \cdot NSCB \quad (7)$$



where

Δ
 $\$CB =$ cost of spare connectors and boards

Thus, the total spare parts cost per system is

$$SS = [B \cdot \frac{NES}{NESS} \cdot SA + (1-B)\$CB] \cdot TL \cdot \lambda_s \quad (8)$$

In general, the number of IC's per module is independent of the level of integration of the IC's. Therefore, the level of integration of IC's determines the number of modules per system and the major reliability problem is module board, its connectors, and the interconnection scheme. This can be seen in Fig. 3, curve (3) to be the predominant reliability factor. Actual chip failures are insignificant by comparison.

In terms of the level of integration, NG (number of gates per IC) we have

$$SS = [B \cdot \frac{NES}{NESS} \cdot SA + (1-B)\$CB] \cdot TL \cdot \sum_{j=1}^{NI} \lambda_j \quad (9)$$

and substituting for λ_j we get:

$$SS = [B \cdot \frac{NES}{NESS} \cdot SA + (1-B)\$CB] \cdot TL \cdot \sum_{j=1}^{NI} (2.5 \times 10^{-6} \log (NG)_j) \quad (10)$$

In equation (10) NI is a function of the level of integration, NG. To simplify the analysis we assume each subsystem and each system is made up of IC's with the same level of integration, NG: and thus all IC's will have the same failure rate. Then

$$SS = [B \cdot \frac{NES}{NESS} \cdot SA + (1-B)\$CB] \cdot TL \cdot \frac{N}{NG} \cdot 2.5 \times 10^{-6} \log \cdot (NG) \quad (11)$$

Where we assume N is a constant.

To complete the cost of an electronic system, we must be able to determine the repair costs and the initial acquisition cost.

We assume total acquisition cost to be given by

$$NES \cdot \$A = \$DM \cdot MU \cdot NES \cdot NI + \$CA \cdot NES \quad (12)$$

where

$$\$DM = \overset{\Delta}{\text{LSI device manufacturing cost}}$$

Here, \$CA is the total cost, excluding IC cost, of all system components and all assembly, design, fabrication and testing cost. Again if we assume all IC's have approximately the same level of integration then:

$$\$A = \frac{\$DM \cdot MU \cdot N}{NG} + \$CA \quad (13)$$

The total system repair cost \$R is proportional to the total number of failures over the life of the system and will depend on the repair cost of each failed system.

$$NES \cdot \$R = \lambda_s \cdot TL \cdot NES \cdot [B \cdot \$RPL + (1-B) \cdot \$RPR] \quad (14)$$

Where

$$\$RPL = \overset{\Delta}{\text{cost to replace a module}}$$

$$\$RPR = \overset{\Delta}{\text{cost to repair a module}}$$

\$RPL and \$RPR include all costs of repair or replacement other than parts costs which have been included in \$S.

Again assuming all IC's have approximately the same level of integration,

$$SR = [B \cdot SRPL + (1-B) \cdot SRPR] \cdot TL \cdot \frac{N}{NG} \cdot 2.5 \times 10^{-6} \log (NG) \quad (15)$$

The total system cost per gate becomes

$$\begin{aligned} \$TG = \frac{\$T}{N} = & \frac{[B \cdot SRPL + (1-B) \cdot SRPR] \cdot TL}{NG} \cdot 2.5 \times 10^{-6} \log (NG) \\ & + \left(\frac{\$DM \cdot MU}{NG} + \frac{\$CA}{N} \right) \left[1 + \frac{B \cdot NES}{NESS} \cdot TL \cdot \frac{N}{NG} \cdot 2.5 \times 10^{-6} \log (NG) \right] \\ & + TL \frac{(1-B) \cdot \$CB \cdot 2.5 \times 10^{-6} \log (NG)}{NG} \end{aligned} \quad (16)$$

Equation (16) contains the terms of importance related to electronic system cost per gate. Since \$DM, the die manufacturing cost, is a strong function of degree of integration, NG, it is not obvious from equation (16) how \$TG varies with NG.

In the following section, a model for IC chip cost will be developed. The model will allow the estimation of \$DM and its dependence on NG, the integration level. The model will also consider chip design/fab approach in establishing \$DM.

III. MACROSCOPIC MODEL OF INTEGRATED CIRCUIT CHIP COST

A. Basic Assumptions and Background

The design and manufacture of an IC is a costly, time consuming process with hundreds of sequential steps. The difficulty and level of sophistication of the manufacturing process can only be realized by noting the fact that a "small" error in any one of the hundreds of sequential steps may cause total irreversable circuit failure. Thus, in the manufacture of IC's, the manufacturer strives to improve control and reduce errors by use of such things as:

- automated equipment under computer or microprocessor control
- redundancy or fault tolerance in the actual fabrication process (eg. double contacts, flowed glass, thick overcoat passivation, iso-planar oxide isolated structures, etc).
- close supervision and monitoring of all work in process
- increased operator training (use of higher skill levels)
- fault tolerant or process variation tolerant circuit designs.

This analysis is restricted to MOS (metal-oxide-semiconductor) integrated circuits. A general literature search on topics related to the design, fabrication, assembly and testing of MOS integrated circuits is attached to this report as Appendix A. Also, the results of a literature search on topics related to the cost of integrated circuits is attached as Appendix B.

A block diagram showing the major steps in the design and manufacture of an integrated circuit is shown in Figure 4. Each block repre-

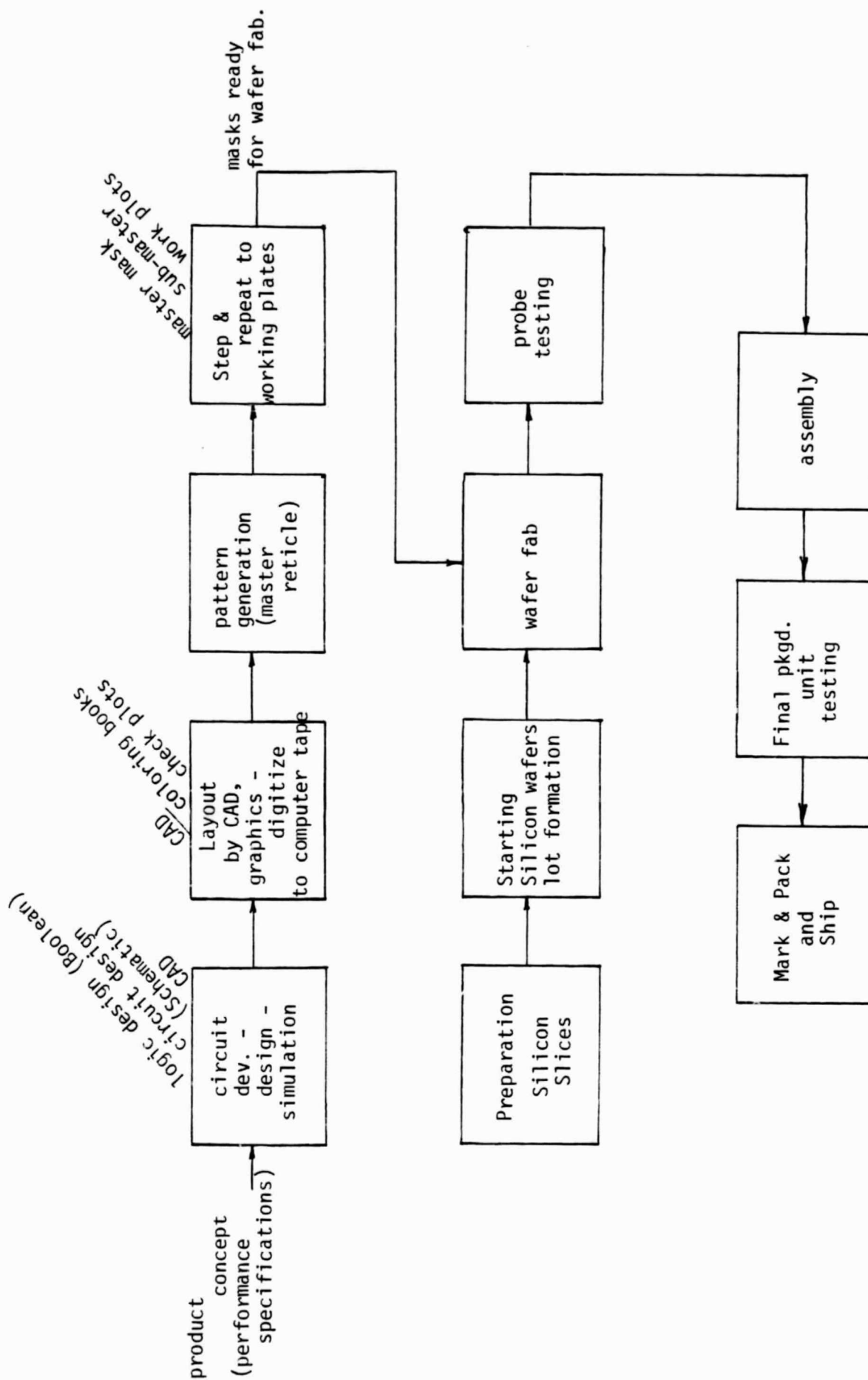


Fig. 4

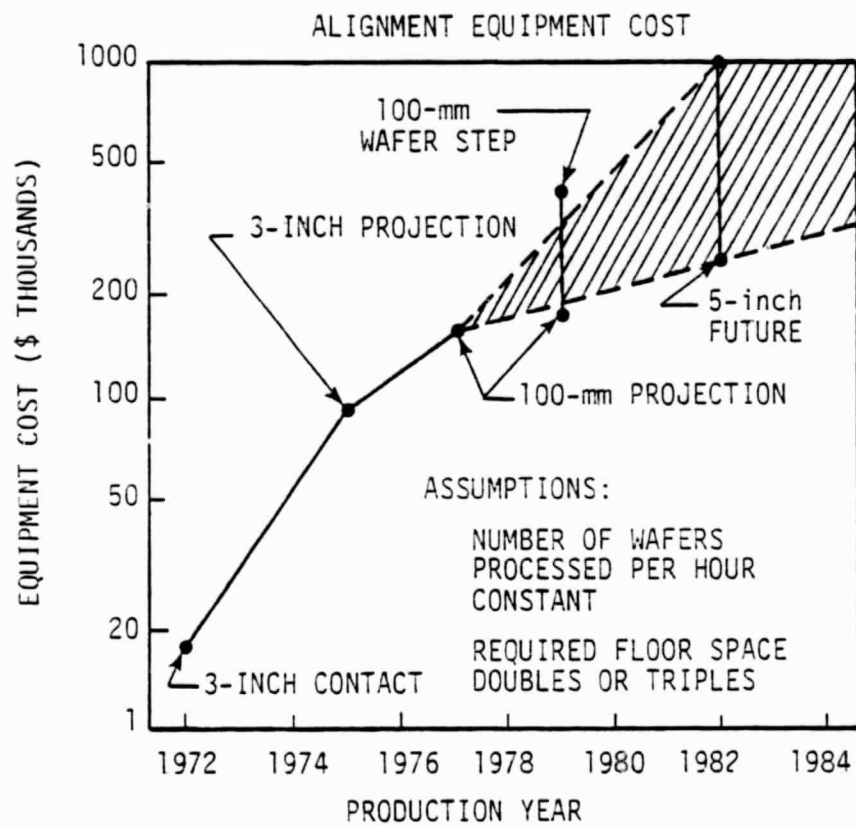


Figure 5

ref. Electronics
Nov. 1978

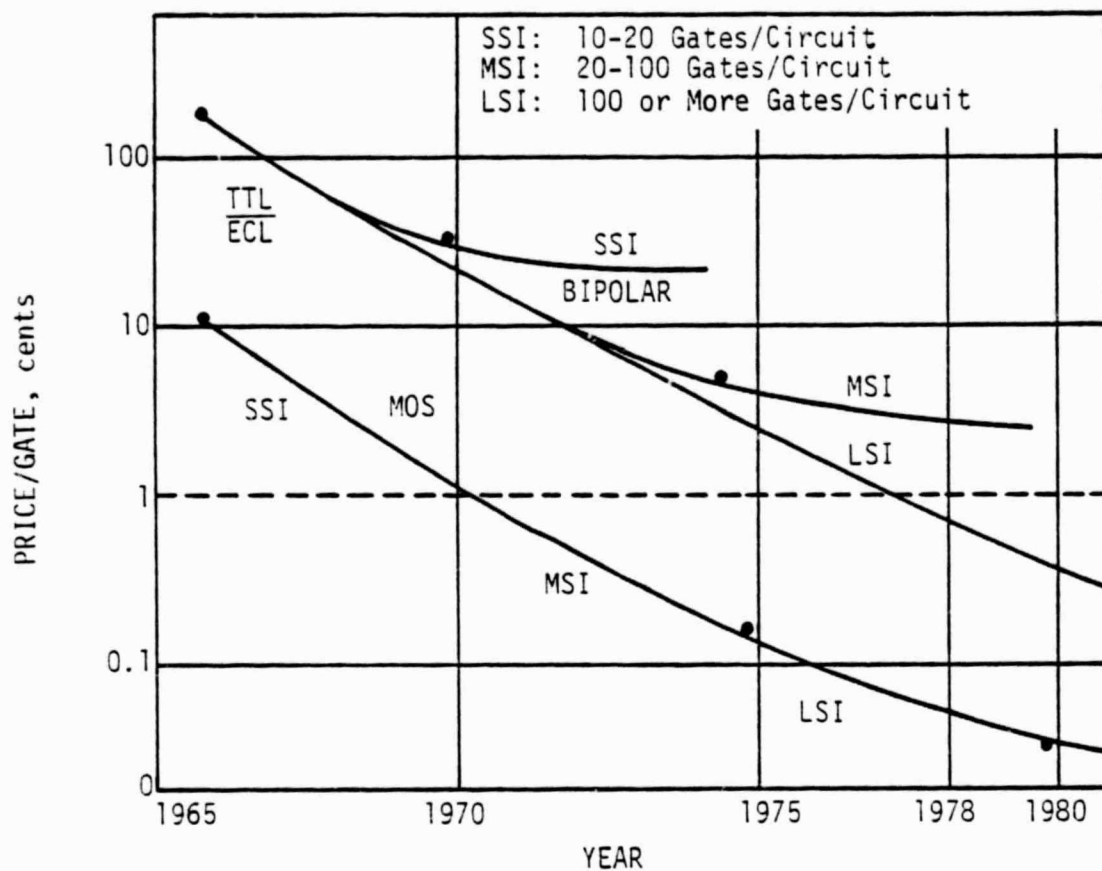
sents considerable detail. Because of the major investment required in capital equipment and high technology personnel in order to manufacture IC's, it would be totally impractical to consider, for example, the low volume manufacture of LSI in a low volume line.

Another major cost is in equipment to manufacture LSI. Growth in alignment equipment costs over the past few years is shown in Figure 5. This is typical of other equipment also.

Improvements in IC technology have permitted higher and higher levels of integration which have resulted in reduced system (which use non-custom LSI) costs as shown in Figure 6. These cost reductions have been possible by the use of high volume coupled with advancing technology. The level of integration has increased as costs have declined at the IC level as shown in Figure 7. For high volume production, the IC cost/gate vs NG is shown in Figures 8 and 9 for different products. Cost is also a strong function of performance as shown in Figure 10.

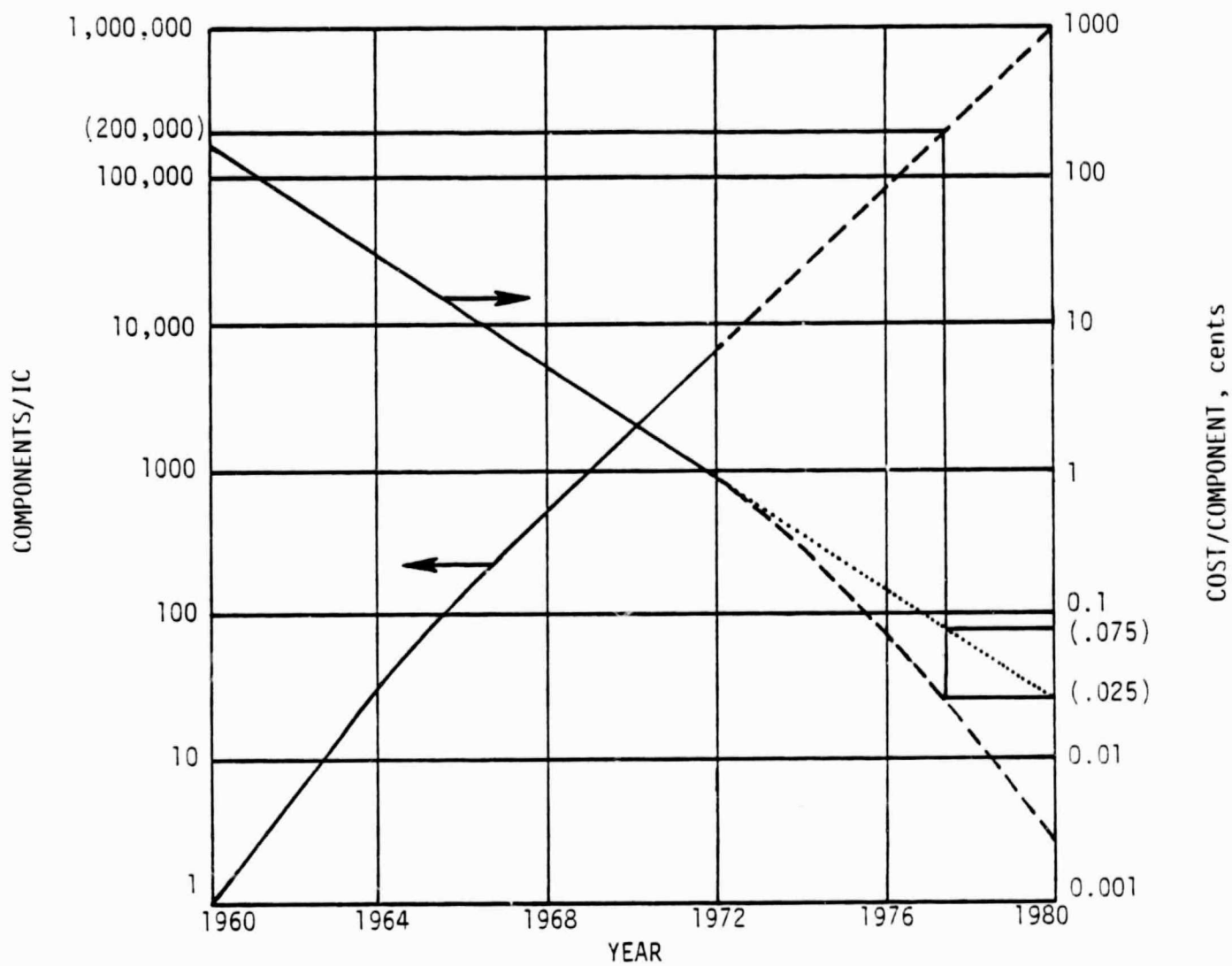
All of the above data is for large volume production. When one considers low volume, custom LSI, the IC cost curves change considerably. The effects of NRE (non Recurring Expense) costs are dominant for very low volume LSI. For example, an LSI logic array could have a \$50,000 NRE cost.

Since equipment costs are so large, the manufacture of low volume, custom LSI is always accomplished in a manufacturing line running a large volume of product. Thus a boundary condition for this work has been established that although the design will allow VLSI custom, the production line will be required to handle a large volume of wafers. This means the production line will be required to handle a large quantity of product types.



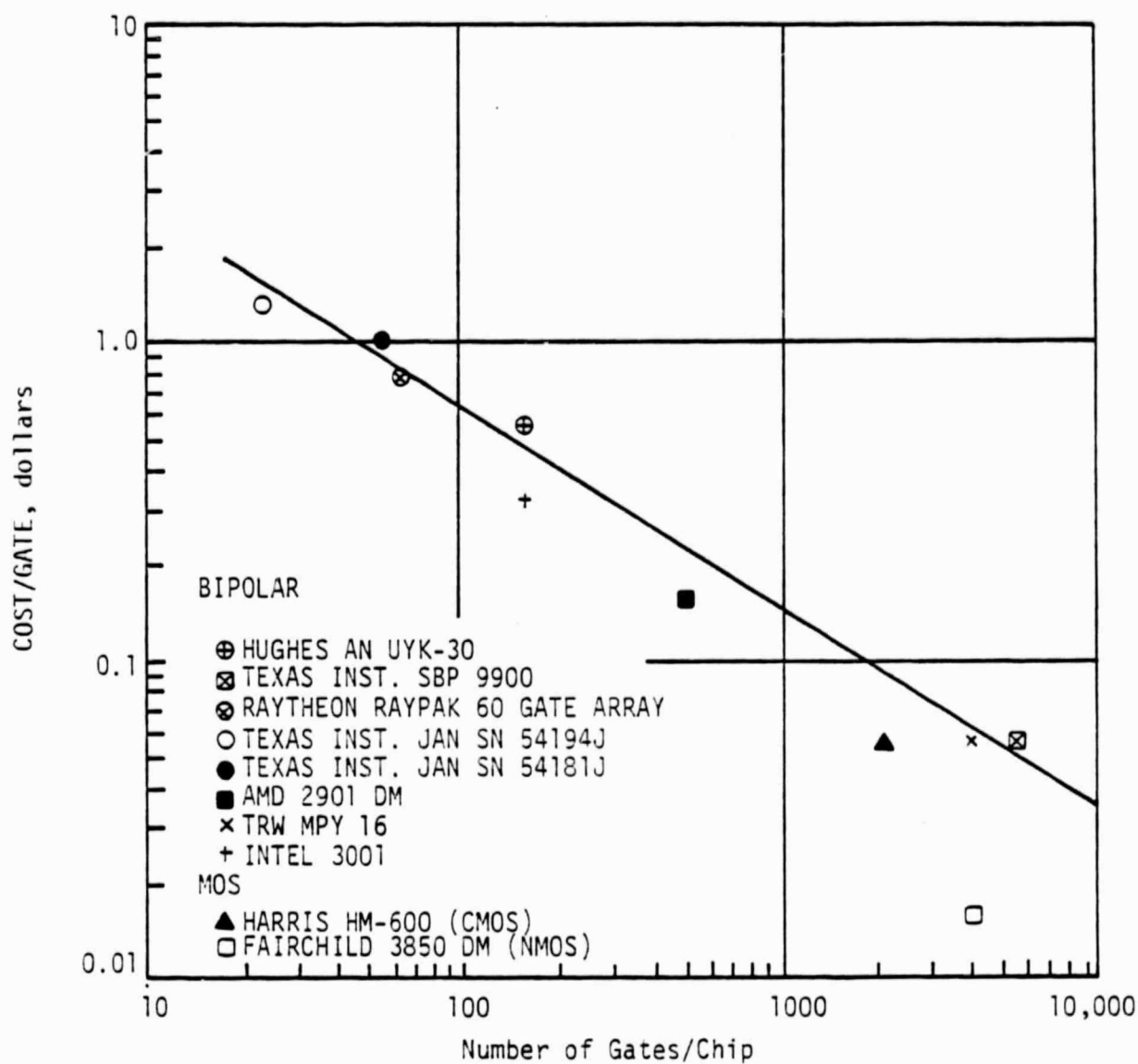
Price/Gate and Level of Integration by Year
for Commercial IC's (ref. 2)

Fig. 6



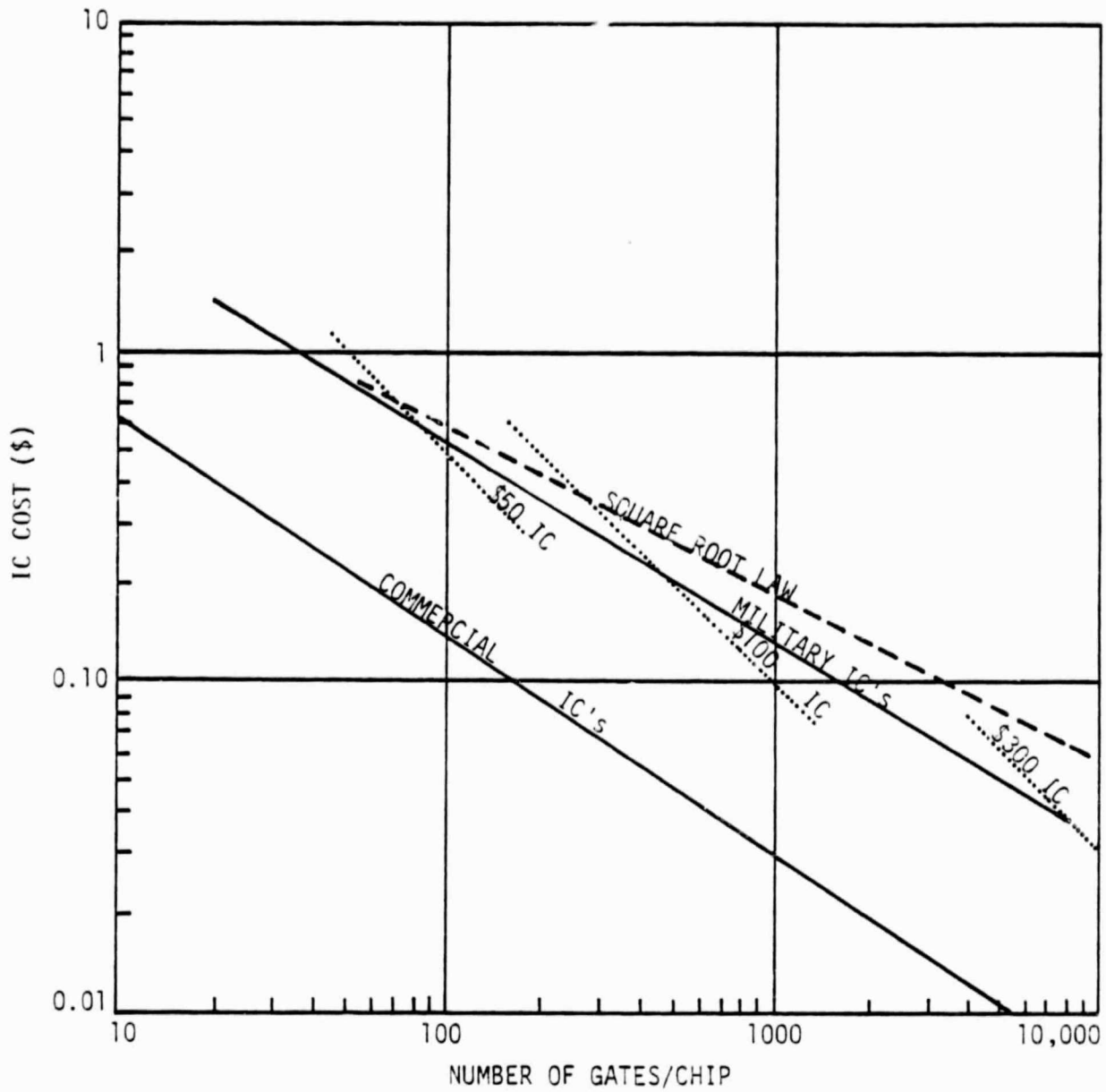
Historical Trends of Components/IC and Cost/Component (ref. 2)

Fig. 7



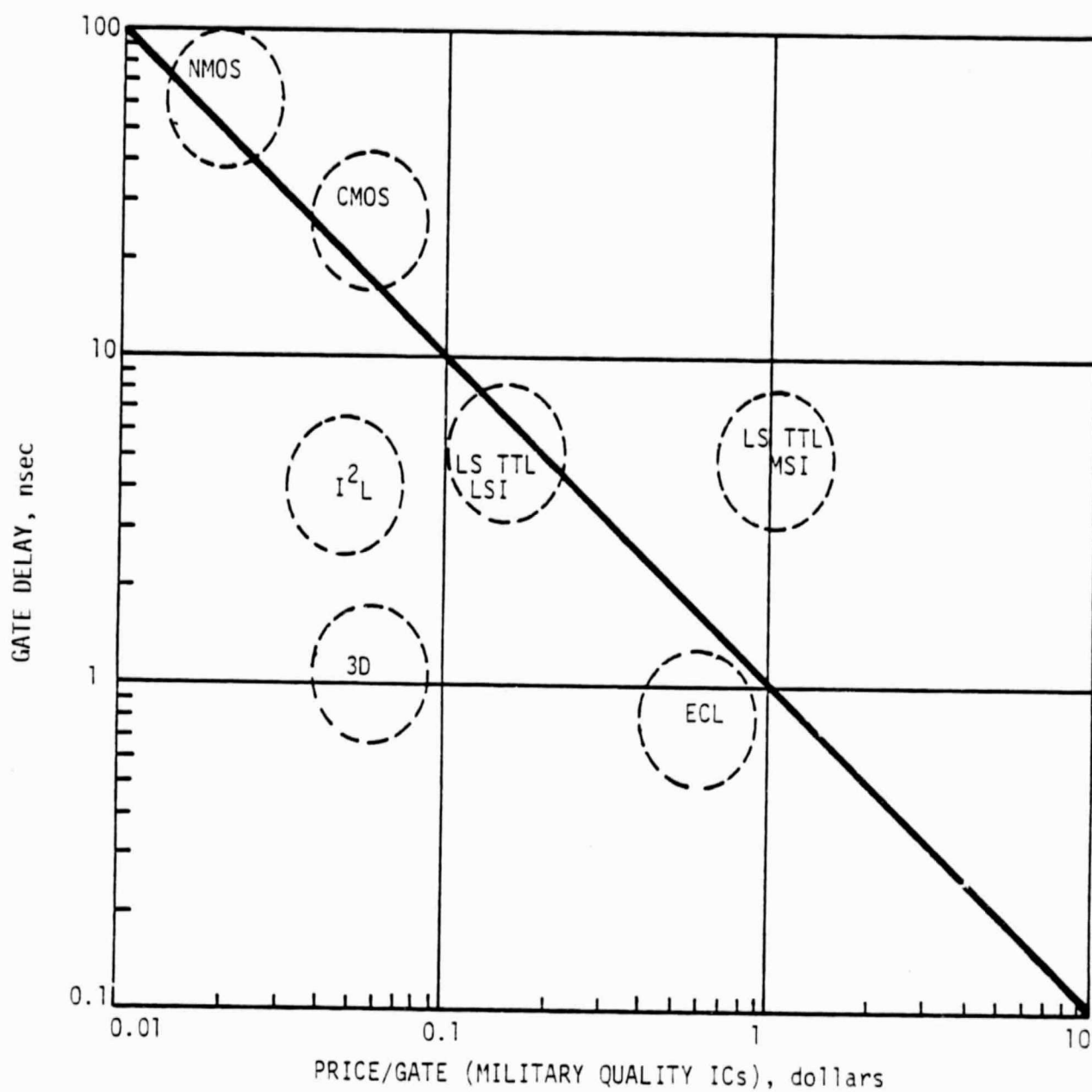
IC Cost/Gate vs. NG
(ref. 2)

Fig. 8



IC Cost/Gate vs. NG
(ref. 2)

Fig. 9



(ref. 2)

Fig. 10

If the manufacturing line is handling a large volume of product, even though this volume is in small runs of custom product, then "some" of the large fixed costs (NRE - non-recurring expense) can be amortized over many volumes of product. In this way, custom manufacturing in wafer fab can approach volume fabrication costs. It will never be the same because of extra paper work involved in tracing lots in the fab line but should be similar to a typical hi-rel line (which requires lot trace) with a large product mix.

In this analysis we assume that the mfg. line is to operate as a "lot traceable" line with a large product mix and perhaps a few different processes in one fab area. We will leave the fab volume as a variable.

To reduce design/layout (d/l) costs we must move toward computer designs with standard gate arrays or standard logic cells which the computer will interconnect. (This is discussed in more detail in the next section.) These generally will result in larger (non-optimum in compaction) die.

Manufacturing yield can easily be related to active die area: [10]

$$Y_D = \prod_{i=1}^n \frac{1}{1 + D_i A_i} = \frac{1}{(1 + D_n A)^n} \quad (17)$$

where

D_i = defects/unit area produced by the i th masking level

A_i = active die area for i th masking level

D_n = average defect density over all n masking levels

A = active die area

n = number of defect producing, yield limiting photo masking operations.

Figure 11

Yield of Die vs. Defect Density for Several Active
Die Areas for a 6 Critical Masking Level Process

$n = 6$

$A = 5$

$A = 10$

$A = 15$

$A = 20$

$A = 30$

Die Yield (%)

92

20

10

D (defects/in²)

0

5

10

15

20

25

30

35

40

45

Figure 12

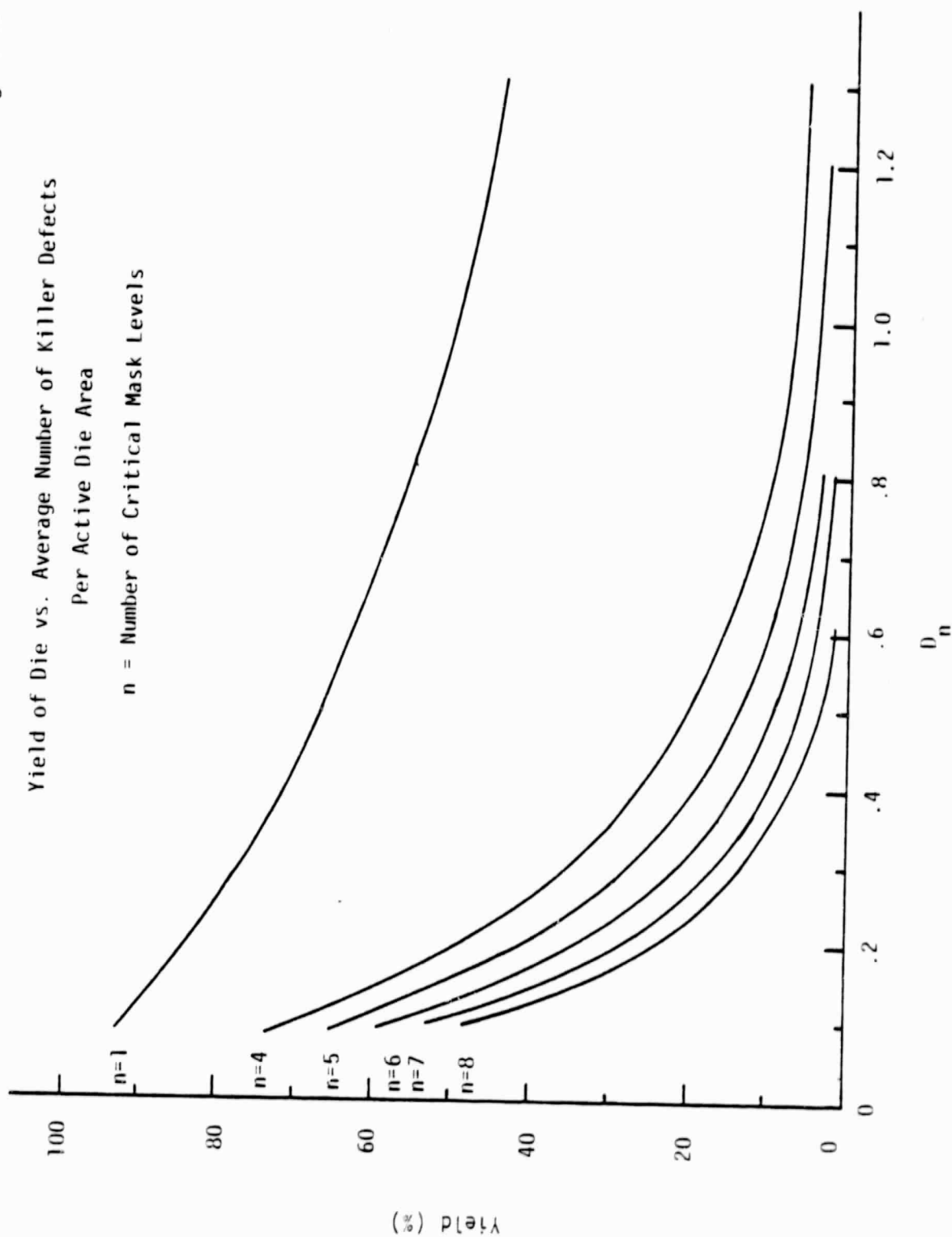
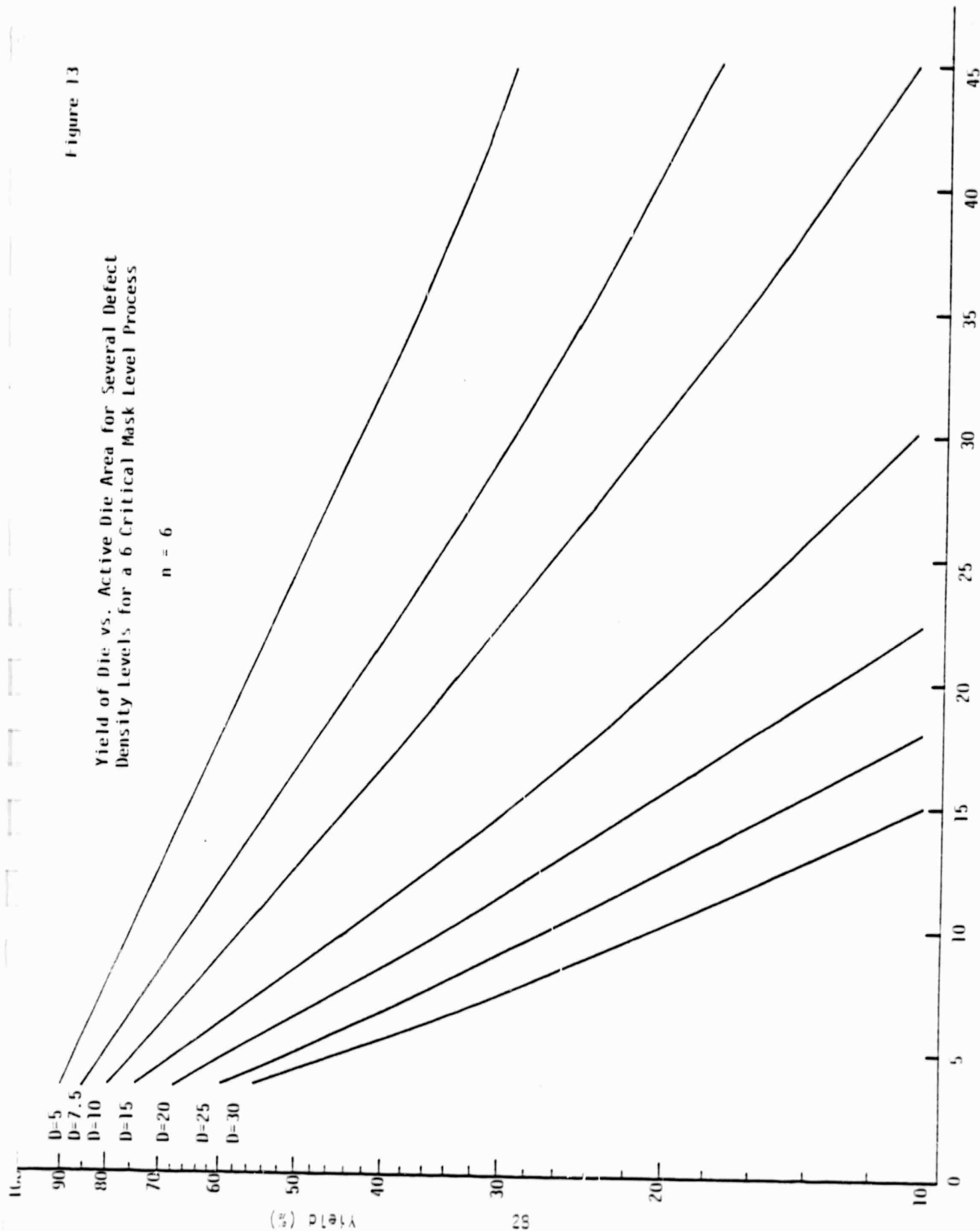


Figure 13

Yield of Die vs. Active Die Area for Several Defect
Density Levels for a 6 Critical Mask Level Process

$n = 6$



SUMMARY OF TYPICAL LSI CHARACTERISTICS

	CLOCK	POWER PER GATE	POWER-DELAY PRODUCT	GATE DELAY	NUMBER OF GATES PER CHIP (NG)	DENSITY ² GATES/mm ²	GATE AREA mm ²	ACTIVE CHIP AREA (mm ²)
TTL	5 MHz	10 mW	100 pJ	10 nsec	75	40	.025	1.875
LS TTL	10	5	30	6	300	40	.025	7.50
I ² _L	5	0.15	1	4	4000	250	.004	16.0
ECL	50	20	20	1	100	30	.033	3.30
PMOS	0.6	2	200	100	4000	150	.0067	26.8
NMOS	3	0.5	20	60	4000	200	.005	20.0
CMOS	3	0.3	10	30	1000	40	.025	25.0

Fig. 14a

Technology	Propagation Delay (ns)	Power-delay product (pJ)	Density		Chip size (mm ²)
			(Devices/mm ²)	(Gates/mm ²)	
High-threshold p-channel metal gate	80	450	150	50	7 x 7
p-channel silicon-gate	30	145	270	90	6.5 x 6.5
n-channel silicon gate	15	45	285	95	6 x 6
n-channel silicon gate depletion-load	12	38	320	107	6 x 6
n-channel double-polysilicon	10	35	525	175	6 x 6
Silicon-gate C-MOS	10	0.5	220	45	5.5 x 5.5
V-MOS D-MOS	5	20	600	225	-
SOS/C-MOS	2 - 5	0.1	650	275	5 x 5
1 ² L (double level)	5 - 50	0.01 - 1	500	150	5.5

MOS/LSI Characteristics

Fig. 14b

(ref. Electronics,
April 1976)

Figure 11 shows plots of equation (17) for different values of active die area vs defect density. Figure 12 shows a plot of equation (17) vs. the $D_n A$ product for various n values and Figure 13 shows yield vs. active die area for various defect densities.

D_n , the defect density (defects per unit area) is a manufacturing and technology problem. At any given time in the fab area for a chosen technology we can assume it is a constant. Die area A_d is determined by the (d/l) cycle, including the device technology.

The relationship of chip area to degree of integration is strongly dependent on several factors:

- layout strategy and efficiency
- levels of interconnect
- active chip area to total chip area ratio
- type of circuit (random logic or memory)

Figure 14 a and b gives the typical characteristics of the more important LSI technologies and an estimated active chip area for the indicated typical NG. This data cannot be used to develop even an empirical relationship between chip area and NG since there is considerable variation in the gate density (or gate area) between processes. Also, the active chip area estimate assumes the entire active circuit is made up of "gate" of average size. This would only be accurate for estimating the size of random logic chips and would not work for memories or other ordered logic.

An empirical equation has been presented by Cunningham and Jaffe relating the die area A_d of MOS memory chips to the number of bits in the memory, N_0 [11]

$$A_d = 1.7 \times 10^{-6} (N_0 + 69N_0^{1/2} + 2400) \text{ in}^2 \quad (18)$$

This equation assumes n-channel silicon-gate technology with standard 6-micrometer design rules and a typical one-transistor cell. In the summation term in parenthesis, the first term, N_0 relates to the total storage-cell area. The second term, $69N_0^{1/2}$, essentially relates to the area required by decoders and sense amplifiers and other areas that depend on column or row length. The third term, 2,400, is a constant because it accounts for unused periphery and circuits, such as buffers, that do not depend on cell area. [11]

For memories, this equation can be generalized somewhat as follows:

$$A_d = A_1 (N_0 + R_1 N_0^{1/2} + R_2) \quad (19)$$

where

A_1 = area of a single memory storage cell

R_1 = coefficient to determine area contribution by row and column decode and sense circuitry

R_2 = coefficient to determine peripheral area contribution

In summary then, the relationship between NG (degree of integration) and die area is different between random logic circuitry and memory. For random logic one can estimate die area by assuming a linear relationship between die area and NG whereas an equation similar to equation (19) must be used for memories. Specifically, in this work, we will assume that for random logic with a large number of gates that the area required for interconnecting gates and peripheral area to reach the bond pads and the area of bond pads is:

$$B_1 \cdot NG \cdot K_p + BP \cdot K_p \cdot (NG)^{1/2} \quad (20)$$

Thus, total die area becomes:

$$A = A_G \cdot NG + B_1 \cdot KP \cdot NG + BP \cdot KP \cdot \sqrt{NG} \quad (21)$$

where

$$\begin{aligned} K_p &= \text{average pins per gate} \\ A_G &= \text{average gate area} \\ BP &= \text{bond area pad} \end{aligned}$$

B. Fabrication Alternatives

There are basically two alternatives to the design and fabrication of custom electronic systems with LSI:

1. Use of full-custom designed LSI
2. Use of semi-custom LSI and standard transistor arrays

Full-custom LSI integrated circuits can offer advantages when the volume of circuits needed or some other parameter can justify the initial high cost of tooling and layout design. In this approach, the IC is unique at all mask levels and therefore can offer the highest performance and/or smallest die size (depending on the design goals).

The volume of integrated circuits needed to amortize a full-custom design depends very strongly on the actual circuit since the initial engineering costs depend heavily on the circuit design and its complexity.

The time required for the design and fabrication phase is often a very important aspect which affects the choice of fabrication alternative. A typical full-custom IC design and layout will take 15 weeks and then another 13 weeks will be needed to obtain finished parts.

A good discussion of the semi-custom alternative to full-custom LSI fabrication has been presented by Edge [7]. In this paper, the cost and fabrication time advantages of the semi-custom approaches are discussed as well as the disadvantages of limited availability of basic chip designs.

Key disadvantages of the single-metal semi-custom approach are the performance, packing density and circuit complexity available. Full-custom MOS LSI is capable of 10 MHZ operation whereas single-metal semi-custom is limited to the 2-5 MHZ range. The relatively small gate arrays available for single-metal semi-custom designs will limit the complexity and packing density achievable using this approach. Packing density differences of 2:1 are common for LSI designs using these two approaches. Double-metal semi-custom has none of the above disadvantages, however, design and fabrication are more complex than single-metal semi-custom.

C. Generalized Model for Chip Cost

In this section, a mathematical model is developed for IC die cost in terms of manufacturing parameters and degree of integration as it is related to die area. The objective is to establish an expression for \$DM as used in equation (16).

Die cost is determined to a large extent by yield. For a fixed volume of product in the manufacturing line, die cost is inversely proportional to yield.

$$SD = \frac{SW}{YD \cdot ND} \quad (22)$$

Where \$W = cost per wafer out of fab

YD = die probe yield

ND = total number of die on a wafer

\$D = cost per good die out of fab

The dependence of \$D on A_d can then be calculated as:

$$\$D = \frac{\$W}{\left(\frac{1}{1 + D_n A_d}\right)^n \frac{\pi d^2}{4A_d}} \quad (23)$$

↘ total number of die of area A_d on a round wafer of diameter d.

$$\$D \propto A_d (1 + D_n \cdot A_d)^n$$

and $\$D \propto A_d (1 + D_n \cdot K_a \cdot A_d)^n$ where $K_a = A/A_d$ (24)

Thus \$D will vary slightly more rapidly than linearly with A_d if D_n is not too large. If D_n is large,

$$\$D \propto A_d^{n+1} \quad (25)$$

and can vary very rapidly as n is typically 6-10. We can express it as

$$\$D \propto A_d^m \quad 1 < m < n+1 \quad (26)$$

For VLSI at today's defect densities of 5-7 defects/in², the term $D_n \cdot A_d \cdot K_a$ would not be much larger than unity as shown by a sample calculation.

Assuming 5 defects/in² and $K_a = .8$:

$$\text{Let } \underbrace{D_n \cdot K_a \cdot A_d}_{D_n} = 1, \text{ then } A_d = \frac{1}{4} \text{ in}^2 = .25 \text{ in}^2 \text{ die}$$

= .5 in x .5 in

about 2x the largest die built today in any volume

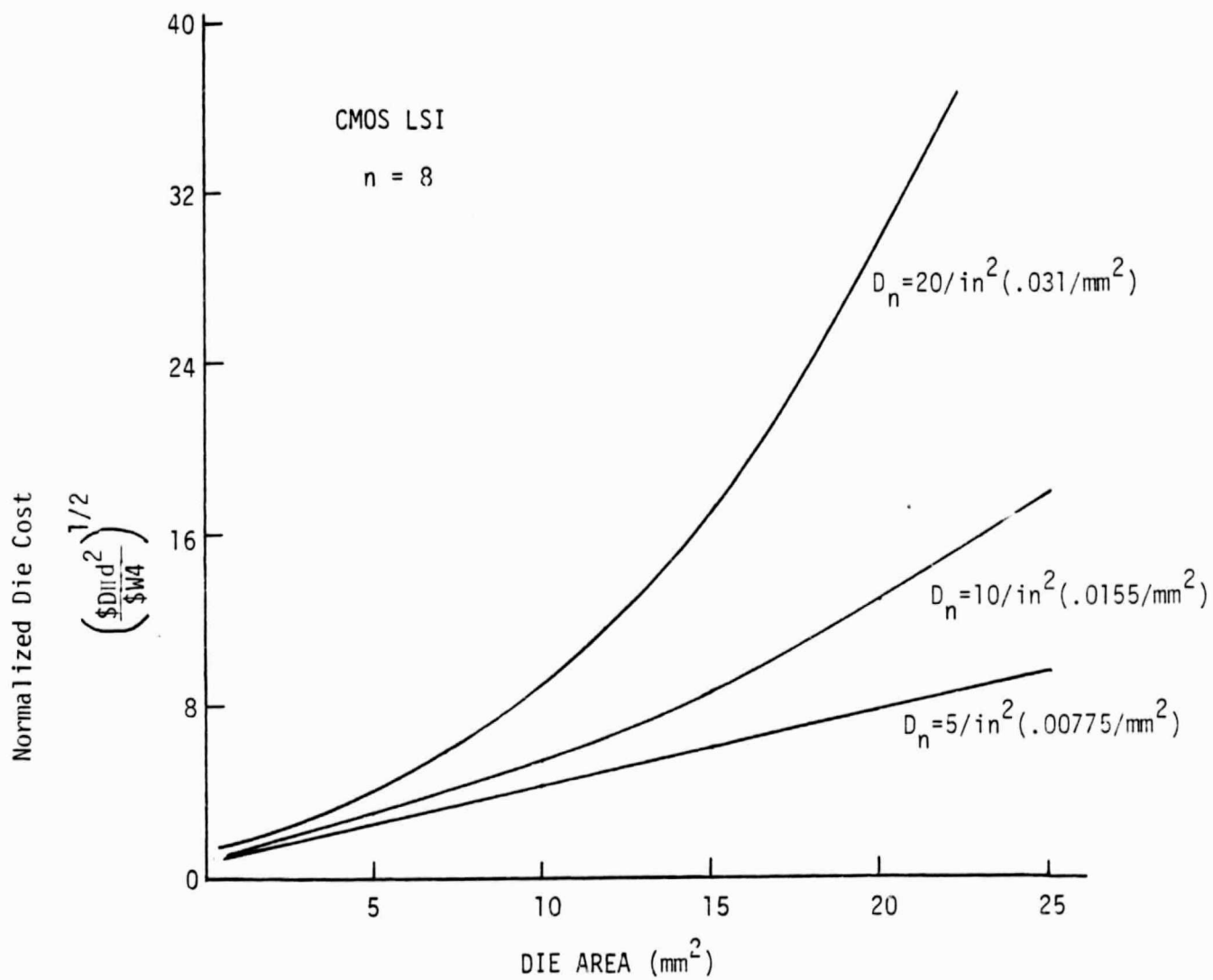


Fig. 15

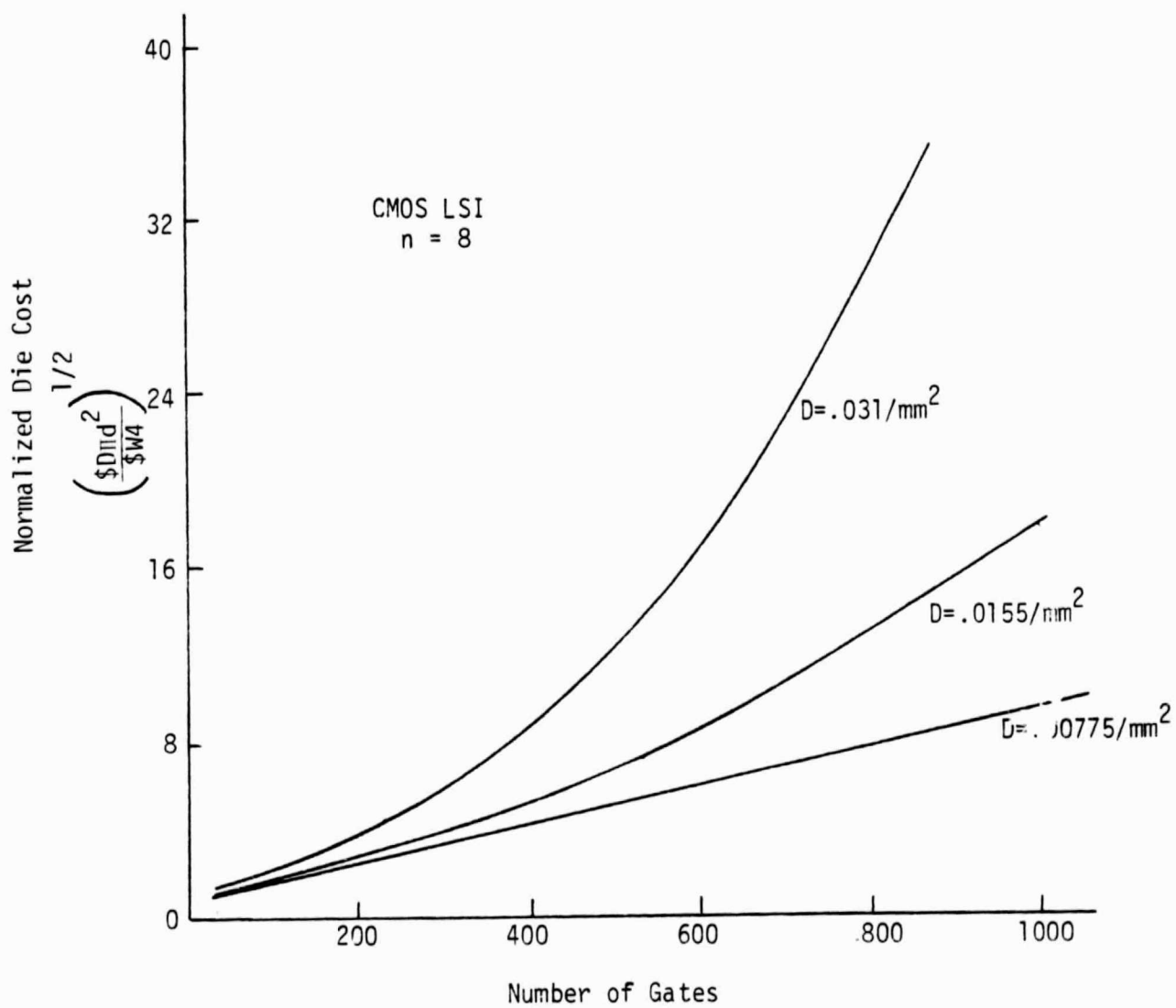


Fig. 16

A die this size would yield (for $n = 5$, $D_n = 5$)

$$Y_d = \frac{1}{(1+D_n A)^n} = 3.1\% \text{ a low yield, high } \$D. \quad (27)$$

For a fixed wafer diameter, d , $\$W$ the wafer fab cost is a constant, independent of die area A . Figure 15 shows how normalized die cost, $\$D$ varies with die area, A . If we assume a CMOS process and a random logic chip, then using $AG=4 \cdot 10^{-5} \text{ in}^2$ from Figure 14 and $A_d = \frac{AG \cdot NG}{K_a} = 5 \cdot 10^{-5} \cdot NG$ we can convert equation (23) into

$$\$D = \frac{\$W}{\left(\frac{1}{1 + D_n [4.0 \times 10^{-5}] NG} \right)^n \left(\frac{\pi d^2}{4 [5.0 \times 10^{-5}] NG} \right)} \quad (28)$$

where D_n is expressed in defects/ in^2 .

Equation (28) is shown plotted in Figure 16 and clearly indicates the effect of degree of integration, NG , on die fab cost. In this figure, die cost has been normalized by wafer fab cost which has been assumed constant. The move toward low volume VLSI will most certainly result in a greatly increased die cost unless $\$W$ is decreased or wafer diameter, d is increased.

Die area is critical to $\$D$; but so is (d/ℓ) cost. For a given level of integration and a fixed set of design rules,

$$\begin{array}{l} \$(d/\ell) \uparrow \text{ as } A_d \downarrow \\ \$D \quad \downarrow \text{ as } A_d \downarrow \end{array} \quad \text{competing roles -}$$

$\$D + \(d/ℓ) must be as low as possible to minimize final die cost. As a

general rule, we want A_d as small as possible for a given level of integration. This tends to increase $\$(d/\ell)$. $\$(D/\ell)$ and $\$D$ can be optimized by use of CAD routing, computer assisted layout, etc. and of course more efficient routing techniques.

The total cost to manufacture an LSI device can be expressed as:

$$\$DM = \frac{\$F}{N_m} + \frac{\$d/\ell}{N_m} + \frac{\$AC}{Y_A \cdot Y_{FT}} + \frac{\$TC}{Y_{FT}} \quad (29)$$

where we define

$\$DM \triangleq$ total manufacturing cost per IC successfully completing manufacture

$\$d/\ell \triangleq$ design/layout cost (fixed NRE)

$\$AC \triangleq$ assembly cost per IC successfully completing manufacture

$\$TC \triangleq$ total test cost per successful IC

$N_m \triangleq$ total number of successful IC's of this type manufactured

$Y_T \triangleq$ total yield = $Y_F \cdot Y_D \cdot Y_A \cdot Y_{FT}$ where

Y_F = wafer fab yield

Y_D = wafer probe yield = $\frac{1}{(1+D_n A)^n}$

Y_A = assembly yield

Y_{FT} = final test yield

$\$F \triangleq$ total cost for fab of all wafers (good & bad) with volume N_m
where $\$F = f(N_m)$

$D_n \triangleq$ average die defect density

$A_d \triangleq$ die area A = active die area

$n \triangleq$ number of critical mask levels

Equation 29 can be rewritten as:

$$\$DM = \frac{\$W}{Y_A \cdot Y_{FT}} \cdot \frac{4A_d}{\pi d^2} (1 + D_n A)^n + \frac{\$d/\ell}{N_m} + \frac{\$AC}{Y_A \cdot Y_{FT}} + \frac{\$TC}{Y_{FT}} \quad (30)$$

where

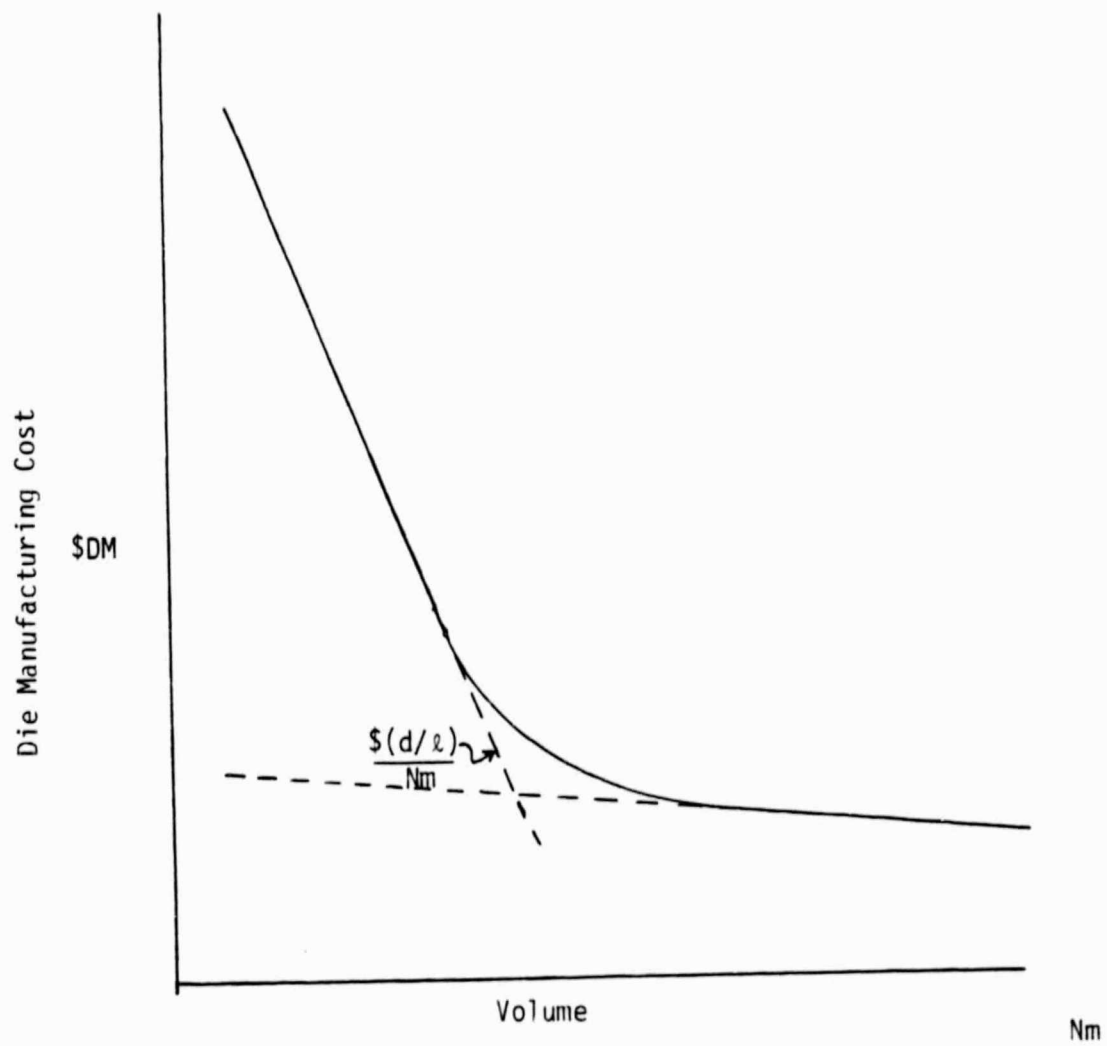
$\$W$ = fab cost per wafer out of fab.

For the condition that N_m is small compared to the total volume of material being processed in the LSI fab line, then $\$W$ will be essentially a constant, independent of N_m . Also, under this condition $\$AC$ and $\$TC$ will be essentially independent of N_m . The sketch in Fig. 17 indicates the relative effect of the $\$(D/L)$ term on costs and thus clearly indicates the cost effect of low volumes.

Calculations of typical costs and a survey of present industry custom LSI manufacturers indicates that the $\$(D/L)$ term dominates for N_m below 20-40 thousand depending on the complexity of the LSI chip. This will be discussed further in Section IV.

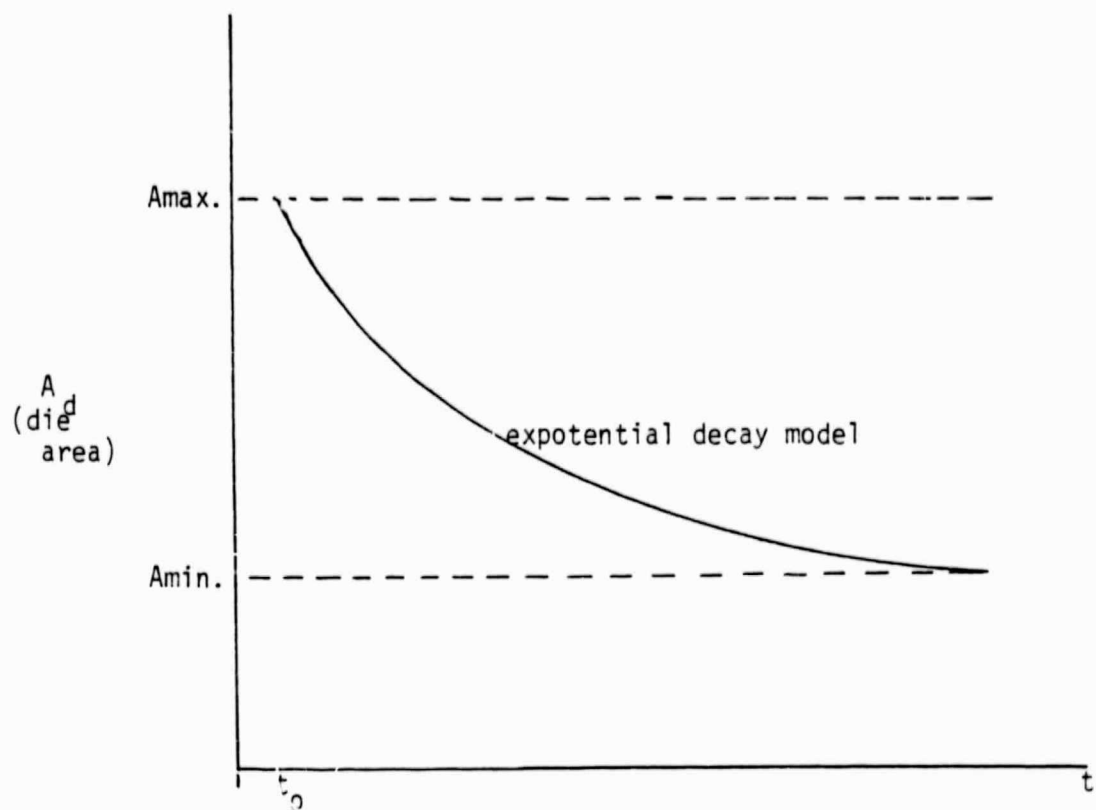
The dependence of equation 30 on die area, A_d , is not obvious until the dependence of the $\$(D/L)$ term is included as well as the $\$TC$ and $\$AC$ terms. In a custom VLSI design/layout, a CAD system is often used to simplify design time and lower costs. Following this CAD layout will usually be a period of manual or semi-manual die size optimization because of the inadequacy of present day CAD software.

A model has been developed to predict die area in terms of three constants or boundary conditions as presented below. We assume the computer generated layout yields a chip of area A_{max} and the absolute theoretical minimum value of die area is A_{min} (zero wasted chip area). The manual labor to reduce die area is assumed to result in an exponential relationship between time spent in optimization vs. area reduction. This is shown in Figure 18.



Device Manufacturing Cost vs Volume

Fig. 17



Die Area vs. Layout Time Optimization

Fig. 18

The model is:

$$A(t) = (A_{\max} - A_{\min}) e^{-\beta t} + A_{\min} \quad (31)$$

The constant β is determined by the efficiency with which the manual effort can reduce A_d from A_{\max} . Of course, A_{\max} is directly affected by the efficiency of the computer in doing a compact layout in the first place. β is dependent of NG. We assume $\beta = \frac{\beta_0}{f \cdot K_p \cdot NG}$ where f is the number of mask levels to be minimized.

The $\$/\ell$ dependence on area can now be established by noting that

$$\$/\ell = \$CR + \$L + \$R \quad (32)$$

where

$\$CR \triangleq$ circuit design cost

$\$L \triangleq$ layout cost

$\$R \triangleq$ reticle fab costs

and

$$\$CR \triangleq \$CE \cdot t_c \quad (33)$$

where

$\$CE \triangleq$ burdened cost per unit time for circuit designer

$t_c \triangleq$ circuit design time

$$\$L = \$CAD \cdot t_{CAD} + \$ML \cdot t_{ML} \quad (34)$$

where

$\$CAD \triangleq$ cost for layout per unit time

$t_{CAD} \triangleq$ CAD layout time

$\$ML$ = cost per unit time for manual layout optimization

t_{ML} = manual layout time

Thus:

$$\$/\ell = \$CE \cdot t_c + \$CAD + t_{CAD} + \$ML \cdot t_{ML} + \$R \quad (35)$$

An expression for t_{ML} is available from equation 31.

$$t_{ML} = -\frac{1}{\beta} \ln \frac{A - A_{min}}{A_{max} - A_{min}} = \frac{1}{\beta} \ln \frac{A_{max} - A_{min}}{A_d - A_{min}} \quad (36)$$

We assume that the circuit design time, t_c , the CAD layout time, t_{CAD} and $\$R$, the reticle cost are related to NG as:

$$t_c = K_1 \cdot K_p \cdot NG \cdot \left(1 - \frac{1}{\sqrt{NG}}\right) \quad (37)$$

$$t_{CAD} = K_p \cdot NG \cdot [\ln(NG) \cdot (K_{21} + K_{22} \cdot K_p) + K_{23} \cdot n_r] \quad (38)$$

$$\text{and } \$R = K_3 \cdot K_p \cdot NG \cdot n_r \quad (39)$$

where $n_r \triangleq$ number of reticles required

These assumptions are most valid for VLSI. For small area die, fixed costs will make t_c , t_{CAD} and $\$R$ essentially independent of NG.

Thus for VLSI,

$$\begin{aligned} \$/\ell = & \$CE \cdot K_1 \cdot K_p \cdot NG \cdot \left(1 - \frac{1}{\sqrt{NG}}\right) + \$CAD \cdot K_p \cdot NG \cdot [\ln(NG) \cdot (K_{21} + K_{22} \cdot K_p) + K_{23} \cdot n_r] + \\ & K_3 \cdot K_p \cdot NG \cdot n_r + \frac{\$ML \cdot f \cdot K_p \cdot NG}{\beta_0} \ln \left(\frac{A_{max} - A_{min}}{A_d - A_{min}} \right) \end{aligned} \quad (40)$$

The costs of making master and working photolithography masks are assumed to be contained in the previous \$W term. The reticle fab costs are assumed to be contained in the \$R term. The reticle fab costs are assumed to contain all costs to go from the layout, however, it is done to the printed reticles. For a computer-aided layout done on a CAD system, the major cost of reticle generation, (for VLSI), will be the time required on a pattern generator to generate a circuit of complexity $f \cdot K_p \cdot NG$. The assumption that $SR = f \cdot K_p \cdot NG$ will be valid under these conditions.

The constants K_1 , K_{21} , K_{22} , K_{23} , and K_3 must be obtained by experience curves and will be highly dependent on the LSI manufacturer, the labor skills and equipment available. They will also depend strongly on the design fabrication approach chosen. For example, the constants will be significantly smaller for a "semi-custom" design where only the design of one or two mask levels is involved.

To complete the present model for cost we must develop the dependence of \$AC and \$TC on level of integration, NG, or die area, A_d . The die assembly cost will be composed of a fixed cost related to processing a die through the assembly operation and other cost components which will vary with die area and NG to some extent. A complete assembly operation, and test sequence is shown in Figure 19. Those assembly operations which have some dependence on die area are:

- wafer scribe
- optical inspection prior to die attach

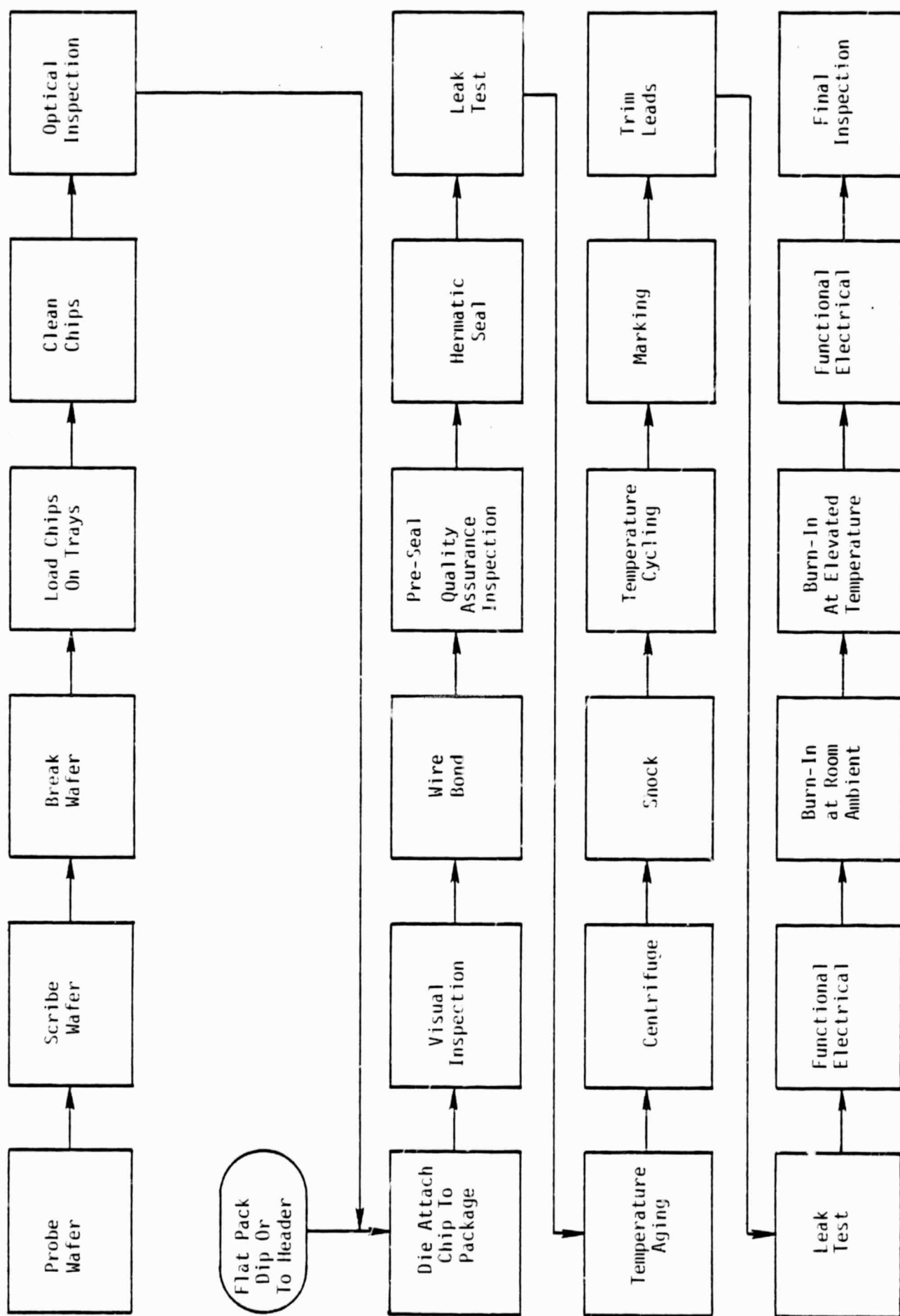


Figure 19. Integrated circuit chip packaging and testing sequence.

The area dependence of the rest of the operations is small and depends mostly on the number of pins on the chip package or the number of bond pads on the chip. The level of integration is in general related to the square of the number of pin-outs. The overall assembly cost of an IC is dominated by the number of bonds required, the package cost and fixed labor costs and overhead. For this analysis, it is assumed that the assembly cost, \$AC, is proportional to $K_p \sqrt{NG}$.

The testing cost of complex IC's is a complicated function of many factors. The dominant factors are

- equipment costs (NRE)
- labor
- circuit complexity and design which determines test times

The number of gates, NG, enters the cost function in that more complex functions are more difficult to test and test time increases. Test time is more dependent on the number of pins on the IC package than on actual die area. In a volume testing situation, the cost \$TC will be totally determined by test time. [12]

In this analysis it will be assumed that the number of pins will determine test cost and that the test cost \$TC varies as $K_p \sqrt{NG}$.

Equation (30) along with equation (40) can now be used to estimate \$DM vs A_d . Inserting equation (21) to eliminate die area and express the cost \$DM in terms of the level of integration we get:

$$\begin{aligned}
\$DM = & \frac{\$W}{Y_A \cdot Y_{FT}} \cdot \frac{4[A_G \cdot NG + B \cdot K_p \cdot NG + BP \cdot K_p \cdot \sqrt{NG}]}{\pi d^2} \cdot \\
& \left(1 + D_n \cdot K_a \cdot [A_G \cdot NG + B_1 \cdot K_p \cdot NG + BP \cdot K_p \cdot \sqrt{NG}]\right)^n + \\
& K_p \cdot \frac{NG}{N_m} \cdot [\$CE \cdot (1 - \frac{1}{\sqrt{NG}}) \cdot K_1 + \$CAD [1n(NG)(K_{21} + K_{22} \cdot K_p) + K_{23} \cdot n_r] + \\
& K_3 \cdot n_r] + K_p \cdot f \cdot \frac{\$ML \cdot NG}{\$o \cdot N_m} \ln\left(\frac{B_1^{mx}/B_1^{mn} - 1}{B_1/B_1^{mn} - 1}\right) + \frac{\$AC}{Y_A Y_{FT}} + \frac{\$TC}{Y_{FT}} \quad (41)
\end{aligned}$$

where:

$K_p \cdot NG \cdot B_1^{mx}$ = routing area maximum (before hand optimization of routing)

$K_p \cdot NG \cdot B_1^{mn}$ = theoretical minimum routing area

f = number of critical mask levels which are hand optimized to reduce layout area

The number, N_m , of IC chips manufactured of any one type is mainly the product of the number of electronic systems, NES, and the number of applications of the chip per system, NA.

$$N_m = NA \cdot NES \cdot [1 + B \cdot \frac{NES}{NESS} \cdot TL \cdot \frac{N}{NG} \cdot 2.5 \cdot 10^{-6} \cdot \log(NG)] \quad (42)$$

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IV. DIE & SYSTEM COST CURVES

A. Introduction

In this section we examine briefly the values of \$DM and \$TG vs level of integration, NG. In order to do the analysis we must make assumptions which provide the necessary constants in equation (16) and (41). Specific values will of course vary widely among manufacturers. However, some general trends can be observed.

The basic assumptions are given in Section IV-B and Section IV-C presents a cost analysis along with a discussion of key results. The basis language computer program which was used in the analysis is presented in Appendix D.

B. Assumptions

To study the dependence of \$DM and \$TG we assume that the LSI chip under consideration is of the order of the 10 gate level or higher since some fundamental assumption in the development of equation (40) will be invalid otherwise. (These assumptions have all been discussed in Section III-A and C.) We also assume that the LSI chips are to be manufactured in an existing volume fabrication area that is typically found in the semiconductor industry today at custom LSI manufacturers (eg. A.M.I.) Four cases will be taken:

- Case I. A full custom, 7 mask level, CMOS LSI design, including all levels from logic design to final packaged parts.
- Case II. Standard off-the-shelf chips for the sake of reference.
- Case III. A semi-custom, 9 mask level CMOS LSI design being a double-metal standard transistor array chip (eg. STAR) and custom design of three mask levels.
- Case IV. A semi-custom, 7 mask level CMOS LSI design being a single-metal standard gate array and custom design of one mask level.

In all cases, \$DM/NG vs NG and \$TG vs NG will be presented.

Case I: Full custom CMOS LSI

We assume:

$$AG = .025 \text{ mm}^2 \text{ (40 gates/mm}^2\text{)}$$

$$d = 100 \text{ mm}$$

$$D_n = 10 \text{ defects/in}^2 = .0155 \text{ defects/mm}^2$$

$$K_A = .8$$

$$\$W = \$200.00, Y_A = .95, Y_{FT} = .90$$

$$K_p = 3$$

$$B_{l_{mn}} < B_l \leq B_{l_{mx}}, B \text{ adjusted for minimum } \$TG$$

$$BP = .0375 \text{ mm}^2$$

$$\$CE = \$15.00/\text{hr}$$

$$K_l = 1 \text{ hr/gate-pin}$$

$$\$CAD = \$220/\text{hr}$$

$$K_{21} = 1.4 \cdot 10^{-2}, K_{22} = 7.0 \cdot 10^{-4}, K_{23} = 1.8 \cdot 10^{-2}$$

$$K_3 = \$1/\text{gate-pin}$$

$$\text{\$ML} = \$10.00/\text{hr}$$

$$\beta_0 = 3 \text{ gate-pin-lev/hr}$$

$$B_{1mx}/B_{1mn} = 4$$

$$B_{1mn} = \frac{AG}{2 \cdot K_p}$$

$$\text{\$AC} = \$0.10 \cdot K_p \cdot \sqrt{NG}$$

$$\text{\$T} = \$0.20 \cdot K_p \cdot \sqrt{NG}$$

$$\text{\$RPL} = \$200 + \$2 \cdot K_p \cdot \sqrt{N} \cdot (1 + \sqrt{\frac{NES}{NESS}})$$

$$\text{\$RPR} = \text{\$RPL} + \frac{\text{\$CA}}{10} \cdot \frac{NES}{NESS}$$

$$B = .05$$

$$TL = 45,000 \text{ hr}$$

$$MU = 2$$

$$f = 6$$

$$NA = 1$$

$$\begin{aligned} \text{\$CB} = \$50.00, \text{\$CA} = & \frac{N}{NG} \cdot \frac{K_c}{N_m} \cdot \left\{ \text{\$CE} \cdot K_1 \cdot \left(1 - \frac{1}{\sqrt{NC}}\right) + \text{\$CAD} \cdot [\ln(NC) \cdot (K_{21} + K_{22} \cdot K_c) + \right. \\ & \left. 3 \cdot K_{23} + \frac{\text{\$ML}}{\beta_0} \cdot 2 \ln(3) \right\} + \frac{NESS}{NES} \cdot (2 \cdot K_c + 750 + \frac{5000}{N_m} + \\ & \left. 10 \cdot K_c \cdot \sqrt{NC} \cdot \sqrt{\frac{NESS}{NES}} \right) \end{aligned}$$

$$\text{where } K_c = K_p \sqrt{NG} \text{ pads per chip and}$$

$$NC = \frac{N}{NG} \cdot \frac{NES}{NESS} \text{ IC's per module}$$

$$N = 10,000$$

$$NES = 50$$

$$NESS = NES \cdot \frac{N}{NG}$$

$$n = 6 \text{ (bond pad assumed non-critical masking level)}$$

$$n_r = 7$$

CASE II: Standard CMOS LSI (same as Case I except no charge for \$d/l)

CASE III: Semi-Custom CMOS LSI in double-metal (STAR) $n_r=3$, $n=8$, $f=3$

CASE IV: Semi-Custom CMOS LSI in single-metal

We assume (parameters not listed are same as above)

$$AG = .1 \text{ mm}^2$$

$$B_{1MN} = A_G/K_p$$

$$n = 6$$

$$f = 1$$

$$K_a = .4$$

$$n_r = 1$$

C. Analysis and Results

Figure 21 displays the total system cost per gate for all four cases. As expected, the minimum system cost occurs with the use of standard off-the-shelf IC's with a level of integration of greater than 77 gates per chip. Standard IC's with NG less than 77 can economically be replaced with single-metal semi-custom IC's. Standard IC's with NG less than 55 can be replaced by full-custom IC's. Standard NG's less than 74 can be replaced with double-metal semi-custom IC's. For example, a system with standard IC's of NG=22 could be replaced with a system with double-metal IC's of NG=630 for one-half the system cost. This in spite of the fact that only 53 copies of each IC type will be produced at a cost of over \$4,000 per individual chip.

The benefit-to-cost ratio (B/C) is a popular tool for decision making. Figure 22 displays the B/C for replacing standard MSI and SSI devices with

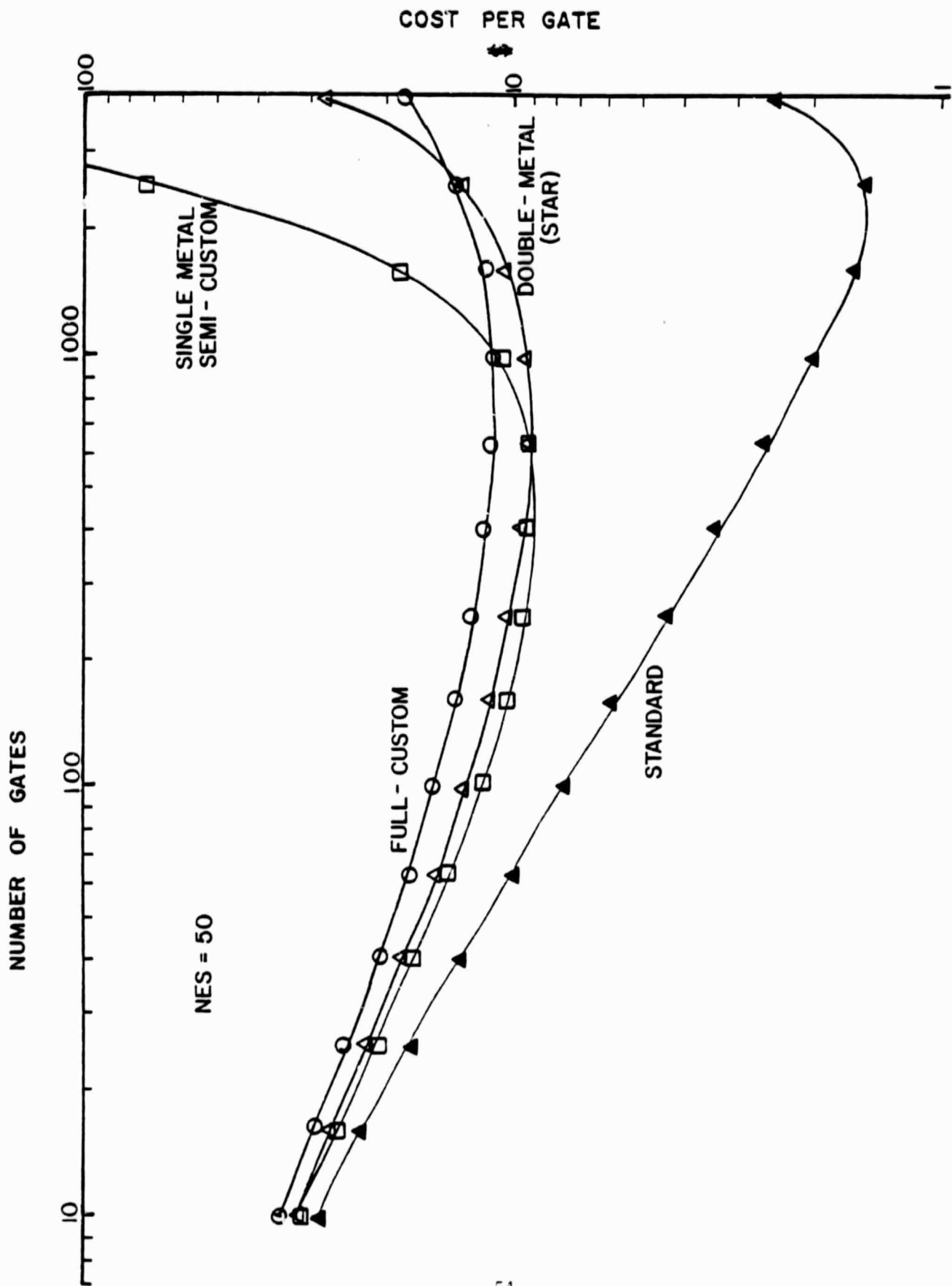


FIGURE 20. COST PER GATE vs NUMBER OF GATES (50 SYSTEMS).

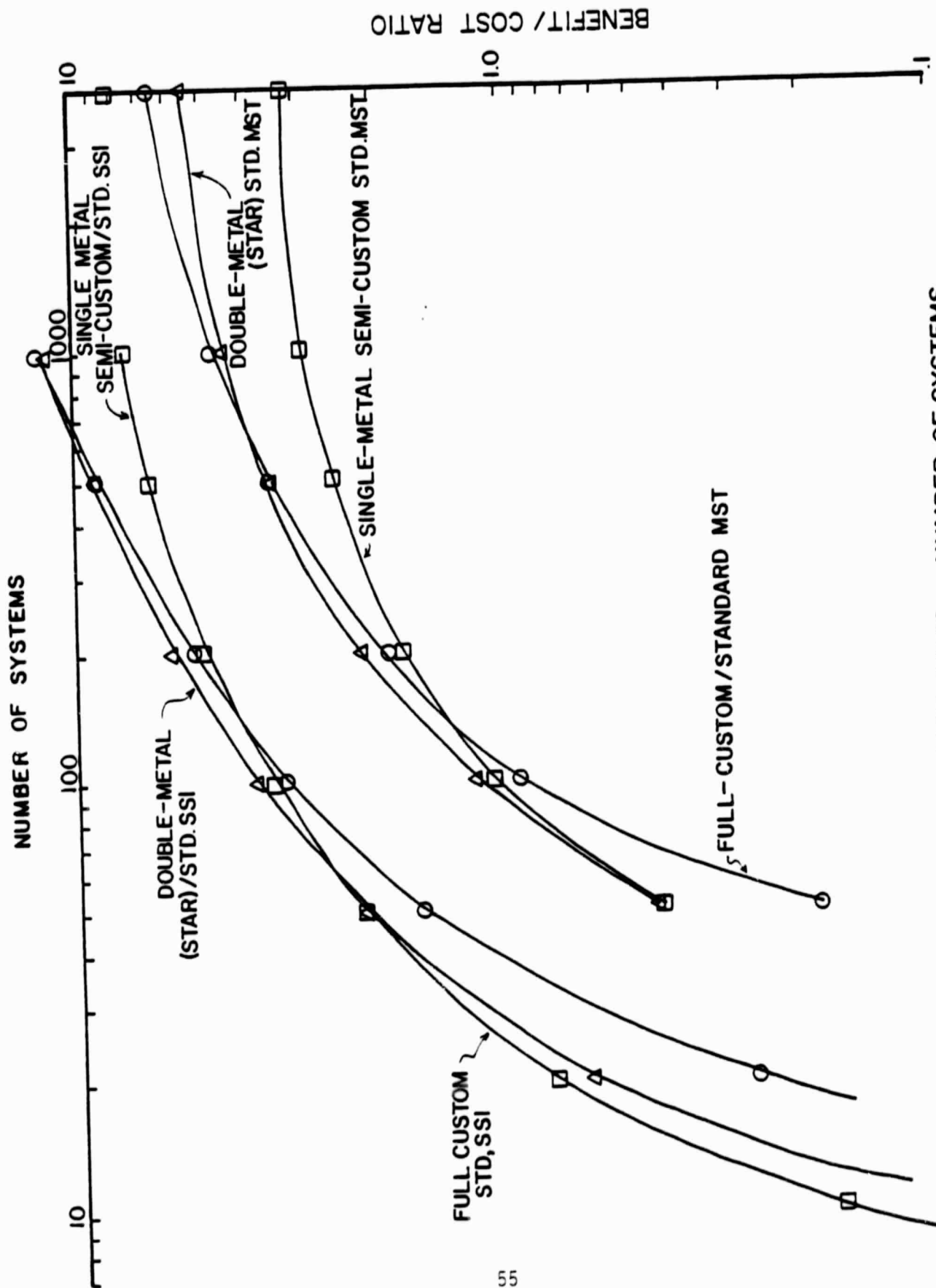


FIGURE 21. BENEFIT TO COST RATIO vs NUMBER OF SYSTEMS.

NUMBER OF SYSTEMS

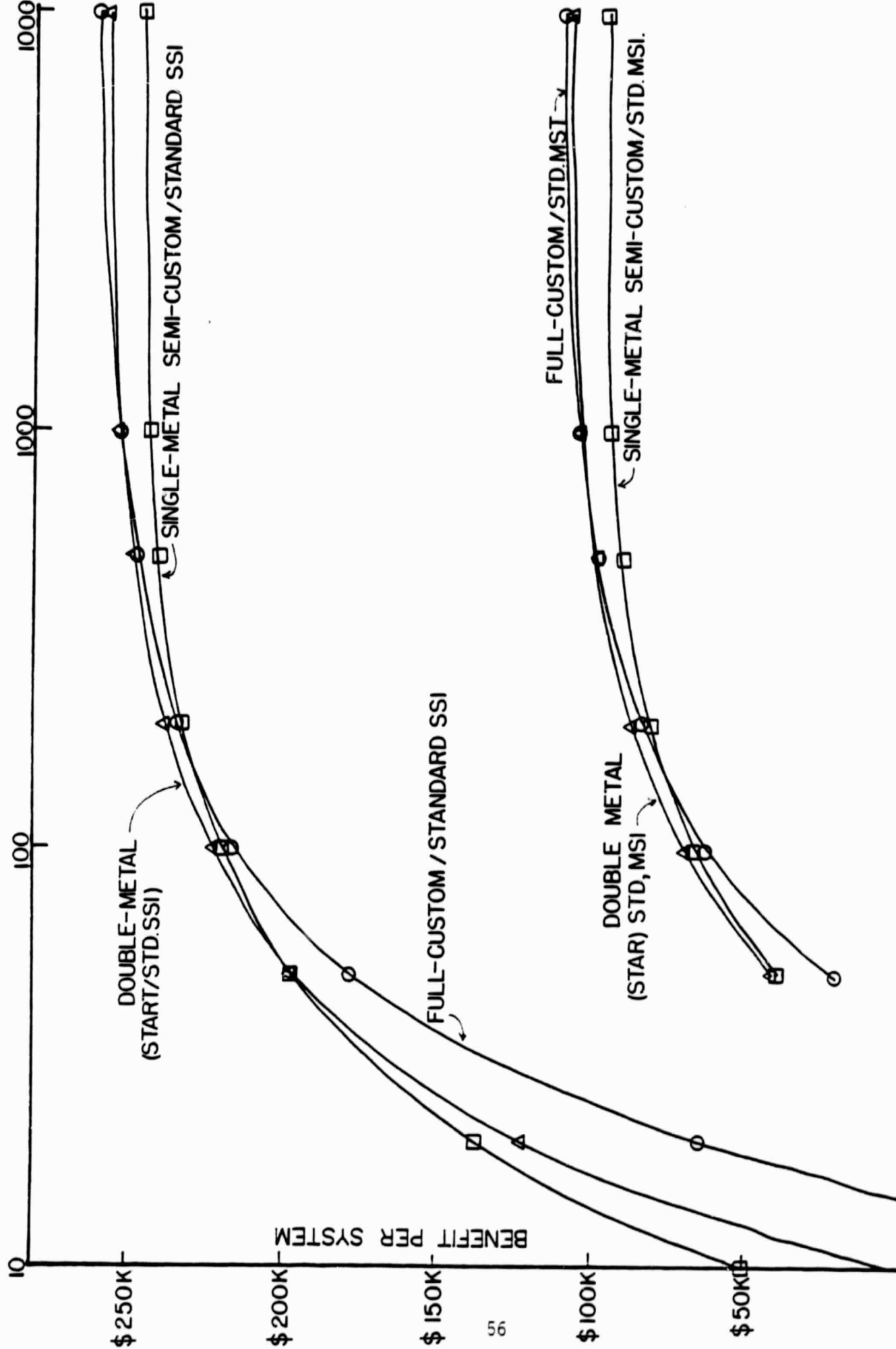


FIGURE 22. BENEFIT PER SYSTEM vs NUMBER OF SYSTEMS.

the various custom device types. Note that a B/C of 1 represents the break even point. B/C is plotted as a function of the desired number of electronic systems where each custom design is used only once per system. Below 5 systems standard SSI is more economical than any custom approach. For 5 to 45 systems, single-metal semi-custom is more economical than standard SSI but not standard MSI. From 45 to 500 systems, double-metal semi-custom STAR devices are the least expensive approach. For greater than 500 systems, full-custom devices are the best choice.

Figure 23 displays the actual cost savings per system relevant to the B/C plotted in Figure 22.

REFERENCES

- [1] G. E. Moore, "Progress in Digital Electronics," Proceedings of the International Electron Devices Meeting, Washington, D.C., (December 1975).
- [2] G. W. Preston, "Large Scale Integrated Circuits For Military Application," I.D.A. Report No. HQ-76-18885, Paper No. P-1244, (May 1977.)
- [3] J. Hohmann, "The Economics of Custom MOS-LSI For Low-Volume Users," Control Engineering, (March 1972.)
- [4] T. P. Kabaservice, "Applied Microelectronics," Chapter 1, pg. 22, West Publishing Co., (1978.)
- [5] G. Sideris, "Custom LSI fades into background," Electronics, (January 10, 1978.)
- [6] R. L. Pritchard, "Trends in Integrated Electronics and Micro-processor Technology," General Electric Report No. 77CRD070, (May 1977.)
- [7] T. M. Edge, "Semicustom and Custom Integrated Circuits and the Standard Transistor Array Radix (STAR)," National Aeronautics and Space Administration, George C. Marshall Space Flight Center, Alabama, RTOP 506-18-31, (1978.)
- [8] J. C. Cluley, "Electronic Equipment Reliability," Halsted Press, (1974.)
- [9] RADC Reliability Handbook and Mil. Std. 217B.
- [10] A. Glaser and G. Subak-Sharpe, Integrated Circuit Engineering, Addison-Wesley, (1977,) pp. 769-795.
- [11] J. Cunnigham and J. Jaffe, "Insight into RAM costs aids memory-system design," Electronics, (December 11, 1975.)
- [12] C. Chrones, "Calculating the cost of testing LSI Chips," Electronics, (January 5, 1978,) pg. 171.

APPENDIX A

APPENDIX A

- "High-yield processing for fixed-interconnect LSI arrays," Sept. 1968, p. 631.
- "Computer-aided design and characterization of digital MOS integrated circuits," Apr. 1969, p. 57.
- Integrated-circuit fabrication; LSI processing techniques. Schmid, Herman, T-MFT 72 Dec 19-31 (1C09).
- Integrated-circuit fabrication - MOS digital integrated circuit manufacturing process; cost reduction of wafer processing part. Seven, Leonce J., ISSCC 74 108-109.
- Klein, T., "Technology and performance of integrated complementary MOS circuits," 1967 NEREM Rec., pp. 168-169.
- "An Overview of the New Mask-Making System," F. L. Howland and K. M. Poole, November 1970, p. 1997.
- "Computer Systems for Pattern Generator Control," A. G. Gross, J. Raamot and Mrs. S. B. Watkins, November 1970, p. 2011.
- "The Primary Pattern Generator:
Introduction, K. M. Poole, p. 2031
Part I--Optical Design, M. J. Cowan, D. R. Herriott, A. M. Johnson and A. Zacharias, p. 2033
Part II--Mechanical Design, G. J. W. Kossyk, J. P. Laico, L. Rongved and J. W. Stafford, p. 2043
Part III--The Control System, P. G. Dowd, M. J. Cowan, P. E. Rosenfeld and A. Zacharias, p. 2061
Part IV--The Alignment and Performance Evaluation, A. M. Johnson and A. Zacharias, p. 2069.
November 1970.
- "The Electron Beam Pattern Generator," W. Samaroo, J. Raamot, P. Parry and G. Robertson, November 1970, p. 2077.
- "Advances in Computer Generation of Master Artwork for Microminiature Circuits, P. R. Strickland and B. J. Crawford, July, p. 31.
- Economic Considerations in IC Testing, Gary Strong, Mar. p. 52.

Integrated Circuit Manufacturing--Circa 1977, R. M. Burger, R. P. Donovan, Oct. p. 58.

Computer-Aided Design for Photomask Production, F. K. Richardson, G. L. Resor, June, p. 60.

Computerized Mask Making for Complex Memory Chips, J. McCracken, C. Johnson, Sept., p. 36.

Efficiency and Programming of Automatic Artwork Generators, A. K. Chitayat, J. Lauria, Nov., p. 41.

Expected Levels of Circuit Integration in the Early 70's, Bernard Reich, Feb., p. 60.

Integrated Circuits for the Industrial World, Lloyd Maul, Sept., p. 43.

Plastic Semiconductor Devices and Integrated Cricuits for Military Applications, Bernard Reich, Jan., p. 53.

An Overview of Photomasking Technology in the Past Decade, Austin J. O'Malley, June, p. 57.

Automatic Mask Alignment in MOS/LSI Processing, K. Clark, Feb., p. 48.

Computer-Controlled Artwork Generation at 10X, Richard Cast, Feb., p. 29.

Monitoring Needs in the Microelectronics Industry of the Fugure, R. P. Riegert, Dec., p. 58.

Silicon Wafer Technology--State of the Art, J. T. Law, Jan., p. 25.

Large IC Chip Impact Analysis and Handling Protection, L. K. Karstadt, W. G. Burger, C. M. Hsieh, W. A. Cosgrove, Aug., p. 41.

Low-Cost Interactive Graphics for Solid State Design, David Albert, Feb., p. 44.

Photo-Composition and LSI, Joseph P. Murphy, Gerald Henriksen, Les Woods, Jun., p. 29.

Electron-Beam Microfabrication Equipment for Microcircuit Research and Production, W. R. Livesay, Jun., p. 37.

"The electron beam fabrication of small geometry transistors," Larkin & Matta, 1967-May, p. 491.

"Computer aided transistor design, characterization, & optimization," Bhosh, et.al., 1967-July, p. 705.

- "Physical limitations of MOS structures," M. B. Das, 1969-May, p. 305.
- "Fundamental limitations in microelectronics: I. MOS technology,"
Hoeneisen & Mead, 1972-July, p. 819.
- "Limitations in microelectronics: I. Bipolar technology," Hoeneisen
& Mead, 1972-Aug., p. 891.
- "Interactive scheme for computer simulation of semiconductor devices,"
Seidman & Choo, 1972-Nov., p. 1229.
- A. F. Tasch, Jr. and V. R. Porter: Photomask array placement on
slices in LSI processing, p. 539.
- Schnable, G. L., and Keen, R. S., On Failure Mechanisms in Large-Scale
Integrated Circuits, Advances in Electronics and Electron Physics,
Vol. 30, L. Marton, ed., pp. 79-138. (Academic Press, New York,
1971).
- Geer, Ronald G., Computer-Aided Course Grid Layout Technique For Photo-
masks, The Electronic Manufacturer's Journal, Sept. 1976, p. 65-69.

APPENDIX B

BIBLIOGRAPHY

1. "Analysis of Transmission Lines on Integrated-Circuit Chips", I. Ho & S. Mullack, IEEE Journal of Solid State Circuits, Volume SC-2, Number 4, December 1967, pp. 201-207.
2. "Applying a Composite Model to the IC Yield Problem", R. Warner, Jr., IEEE Journal of Solid State Circuits, Volume SC-9, Number 3, June, 1974, pp. 86-95.
3. "Automatic Artwork Generation for Large Scale Integration", P. Cook & W. Donath, IEEE Journal of Solid State Circuits, Volume SC-2, Number 4, December, 1967, pp. 190-195.
4. "Automatic Test Generation Methods for Large Scale Integrated Logic", E. Jone & C. Mays, IEEE Journal of Solid State Circuits, Volume SC-2, Number 4, December 1967, pp. 221-226.
5. "Beam Lead Sealed-Junction Memory with Minimal Cell Complexity", J. Iwersen & J. Wuorinen, Jr., IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December 1967, pp. 196-200.
6. "Bibliography on Electronic Packaging, II, A", A. Agajanian, Solid State Technology, October 1975, pp. 56-68.
7. "Calculating the Cost of Testing LSI Chips", C. Chrones, Electronics, January 5, 1978, pp. 171-173.
8. "Cheaper LSI Custom Circuits", D. Rolfe, Elektron. Anz., (Germany), Volume 5, Number 10, pp 205-6.
9. "A Circuit-Design Approach for Enhancing the Yield of Complex Iterative Integrated Electronic Subsystems", L. Ragonese, Proceedings of IEEE., December 1964, pp. 1613-1616.
10. "Comparative Advantages of In-house Custom Design of MOS-LSI", I. Williams, Integrated Electronics Packaging & Production Conference 1973: Proceeding of Technical Programme. Brighton, England, October 16-18, 1973, pp. 153-155.
11. "Complex Monolithic Arrays: Some Aspects of Design and Fabrication", C. Phillips & W. Seelbach, IEEE Journal of Solid State Circuits, Volume SC-2, Number 4, December 1967, pp. 156-171.
12. "Control MOS/LSI Yield By Design", Mel Phelps, EDN/EEE, October 15, 1971, pp.21-27.

13. "Cost Reliability Trade Off in an Electronic Module", K. Surendran & K. Chandra, Microelectronics and Reliability, Volume 15, pp. 493-496.
14. "Cost-size Optima of Monolithic Integrated Circuits", B. Murphy, Proceedings of the IEEE, December 1964, pp. 1537-1545.
15. "Current Status of Large Scale Integration Technology", R. Petritz, IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December 1967, pp. 130-146.
16. "Customized LSI", G. Moore, (Session 3D: Large Scale Integration Technology & Its Application to Computer Systems), Paper 3D-1.
17. "Custom LSI Fades into Background.", G. Sideris, Electronics, January 10, 1974, pp. 74-78.
18. "Design Automation for Complex CMOS/LSI HYBRIDS", J. Smiley & P. Ramondetta, Electronic Packaging Products, Volume 17, January 1, 1977, pp. 66-68.
19. "Design Automation Techniques. For Custom LSI Arrays", A. Feller, presented for meeting Paris, France, April 21-22, 1975.
20. "Design Considerations for Integrated Electronic Devices", J. Wallmark, Proceeding of IRE, March 1960, pp. 293-300.
21. "Economic Considerations in the Design and Manufacture of Integrated Circuits", H. Tooker & M. Bodnar, (Western Electric Publication), 1967, pp. 52-61.
22. "Economic Factors in Microelectronics", Applied Microelectronics, pp. 5-29.
23. "The Economics of Custom MOS-LSI for Low-Volume Users", J. Hohmann, Control Engineering, (USA), Volume 19, Number 3, 1972, pp. 58-61.
24. "Evaluation of Technology Options for LSI Processing Elements", P. Verhofstadt, Proceedings of IEEE, Volume 64, Number 6, June 1976, pp. 842-851.
25. "Expansion of CMOS Array Design Techniques", A. Feller & P. Romondetta, NASA CR-150318, March 1977.
26. "High-Speed CMOS-SOS LSI Using Standard Cells", A. Feller & P. Ramondetta, RCA Engineer, Volume 20, Number 4, December-January 1974-1975, pp. 36-40.
27. "High-Volume Production Testing of Linear Integrated Circuits", G. Stetzler & R. Filek, Western Electric Engineer, Volume 20, Number 1, January 1976, pp. 2-9.

28. "High-Yield Processing for Fixed-Interconnect Large-Scaled Integrated Arrays.", A. Dingwall, IEEE Transactions on Electron Devices, Volume ED-15, Number 9, September, 1968, pp. 631-637.
29. "Influence of Epitaxial Mounds on the Yield of Integrated Circuits", T. Yanagawa, IEEE Proceedings, Volume 57, Number 9, September, 1969, pp. 1621-8.
30. "I²L: Today's Versatile Vehicle for Tomorrow's Custom LSI", J. Altstein, EDN, Volume 20, Number 4, February 20, 1975, pp. 148-155.
31. "Impact of Arrays on Digital Systems", R. Rice, IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December 1967, pp. 148-155.
32. "Impact of Implementation Techniques on System Parameters", R. Berg & L. Wald, National Telecommunications Conference, Atlanta, Georgia, November 21-28, 1973, paper 41C.
33. "Implications of LSI", J. Haddad, IEEE Solid-State Circuit Conference, University of Pa., February 13-15, 1974, pp. 50-51.
34. "Improved Triple Diffusion Means Densest ICS Yet", J. Buie, Electronics, August 7, 1975, pp. 101-106.
35. "Insights into RAM Costs Aids Memory-System Design", J. Cunningham & J. Jaffe, Electronics, December 11, 1975, pp. 101-103.
36. "Integrated Circuits", IEEE Spectrum, June 1964, pp. 62-111.
37. "Integrated Circuit Testing", M. Barber & A. Zacharias, Bell Laboratories Record, May 1977, pp. 125-130.
38. "An IC Factory in the New Age---An Overview", P. Wang, Texas Instruments Incorporated publication.
39. "Ion Implantation and HCL Treatment Simplify SOS/CMOS Processing and Slash Leakage Current", H. Mizokami, Electronic Engineer, Number 103, June, 1975, pp. 26-30.
40. "Interconnection/Economic Tradeoffs with LSI", S. Sander & L. Hobbs, Parallel Processor Systems, Technologies and Applications, London, pp. 191-199.
41. "Large Scale Integration of MOS Complex Logic: A Layout Method", A. Weinberger, IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December, 1967, pp. 182-189.

42. "A Low Cost Non-Epitaxial Bipolar LSI Technology Suitable for Application to TTL Circuits", P. Panousis & R. Pritchett, Electron Device Meeting, Washington D.C., December 9-11, 1974, pp. 515-518. Publication by IEEE, Catalog Number 74 CH0906-8ED.
43. "A Low-Power Multiphase Circuit Technique", B. Watkins, IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December, 1967, pp. 213-220.
44. "L.S.I. Circuit Design", I. Hoglund & H. Berg, Computer Aided Design, Volume 8, Number 3, July, 1976, pp. 165-74.
45. "LSI Yield Projections Based Upon Test Pattern Results: An Application to Multilevel Metal Structures", A. Turley & D. Herman, IEEE Transactions on Parts, Hybrids, & Packaging, Volume PHP-10, Number 4, December, 1974, pp. 230-234.
46. Managing Inventories of Low-Volume Station Products: the Computer Approach, R. Chang, Bell Laboratories Record, July/August, 1977, pp. 181-86.
47. "Master Slice Design Concept Based on Master Cells in ESPI-SOS-CMOS Technology, E. Gonauser & H. Herbst, Siemens Forsh Entwicksungsber, Volume 5, Number 6, 1976, pp. 344-349.
48. "Means of Reducing Custom LSI Interconnection Requirements", D. Calhoun & L. McNamee, IEEE Journal of Solid-State Circuits, Volume SC-7, Number 5, October, 1972, pp. 395-404.
49. Mitsubishi Analysis of Selective Oxidation Process, S. Yamazaki, Report by Fairchild, June 1, 1974.
50. Modeling for Synthesis: The Gap Between Intent & Behavior, G. Estrin, Proceeding of the Symposium on Design Automation & Microprocesses, February 24-25, 1977, Publication by IEEE catalog number 77CH1189-0 C.
51. "A New Look at Yield of Integrated Circuits", J. Price, Proceedings of IEEE, August 1970, pp. 1290-91
52. "Packaging of Very LSI Chips", J. Murphy, Electronic Packaging Products, Volume 12, Number 5, May, 1972, pp. 44-60.
53. "Physical Limits in Digital Electronics", R. Keyes, Proceedings of IEEE, Volume 63, Number 5, May, 1973, pp. 740-767.
54. "Polychip Chips: Quick-turnaround Custom Circuit Designs", J. Forster, paper September, 1977, pp. 209-214.
55. "Predicting the Real Costs of Semiconductor-Memory Systems", R. Koppet & I. Maltz, Electronics, November 25, 1976, pp. 117-22.

56. "Quality Assurance Aspects of Custom LSI", J. Flood, AGARD LECTURE SERIES, Number 75, April, 1975.
57. "Recent SOS Technology, Advances and Applications", R. Ronen & F. Micheletti, Solid State Technology, August, 1975, pp. 39-46.
58. "Redundancy for LSI Yield Enhancement", E. Tammaru & J. Angell, IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December, 1967, pp. 172-181.
59. "The Relative Performance and Merits of CMOS Technologies", A. Aitkeen, A. McArthur, Bell Northern Research, Ottawa, Canada, pp. 327-30.
60. "Reliability Characteristics of Various Microcircuit Technologies", M. Klein & H. Lauffenburger, SAE preparation number 770227 for meeting February 28-March 4, 1977.
61. "Research and Development of a Large-Scale Electronic System", S. Houanessian, IEEE Trans.
62. "Screened Multilayer Ceramics for Thick Film Hybrids", T. Ihuchi, IEEE Transactions on Parts, Hybrids, and Packaging, Volume PHP-10, Number 2, June, 1974, pp. 115-119.
63. "Silicon-on-Sapphire Complementary MOS Memory Cells", J. Allison & F. Heiman, IEEE Journal of Solid-State Circuits, Volume SC-2, Number 4, December, 1967, pp. 208-212.
64. "Single-Slice Superhet", W. Peil & R. McFadyier, IEEE Spectrum, March, 1977, pp. 54-57.
65. "What Level Of LSI Is Best For You? G. Moore, Electronics, February 16, 1970, pp. 126-13-.
66. "Yield Analysis of Large Integrated-Chips", A. Gupta & J. Lathrop, IEEE Journal Of Solid-State Circuits, Volume SC-7, Number 5, October, 1972, pp. 389-404.
67. "Yield, Economic, and Logistic Models for Complex Digital Arrays", R. Seeds, paper at Fairchild Semiconductor, Palo Alto, California.

APPENDIX C

BIBLIOGRAPHY

- Abe, H.; Sonobe, Y.; Enomoto, T.; Fukuwatari, H.; and Komiya, H., "Etching Characteristics of Si and Si-Compound by Gas Plasma and Its Application to the Fabrication of MOS-LSI," Journal of the Electrochemical Society, Vol. 120, No. 3, p. 93C, 1973.
- Abe, H. "A New Undercutting Phenomenon in Plasma Etching," Japanese Journal of Applied Physics, Vol. 14, No. 11, pp. 1825-1826, 1975.
- Abe, H.; Nagasawa, K.; Kuramitsu, Y.; Nishioka, K.; Iwama, I.; and Yumazaki, T., "Dried Process with Gas Plasma for Production of Chromium and Chromium Oxide Film Masks," 6th International Congress on Microelectronics, Munich, Germany, p. 3, November 1974.
- Abe, H., "The Application of Gas Plasma to the Fabrication of MOS-LSI," Oyo Buturi (Japan), Vol. 44, Supplement pp. 287-295, 1975.
- Aitken, A.; Poulsen, R. G.; MacAthur, A. T. P.; and White, J. J., "A Fully Plasma Etched-Ion Implanted CMDS Process," 1976 International Electron Device Meeting Technical Digest, pp. 209-213.
- Abe, H.; Nishioka, K.; Tamura, S.; and Nishimoto, A., "Microfabrication of Anti-Reflective Chromium Mask by Gas Plasma," Japanese Journal of Applied Physics, Vol. 15, Supplement 15-1, pp. 25-31, 1976.
- Bathey, J. F., "The Reduction of Photoresist Stripping Rate in an Oxygen Plasma by By-Product Inhibition and Thermal Masses," Journal of the Electrochemical Society, Vol. 124, No. 1, pp. 147-152, 1977.
- Batty, J. F., "Design Criteria for Uniform Reaction Rates in an Oxygen Plasma [Si Wafer Processing]," IEEE Transaction on Electron Devices, Vol. ED-24, No. 2, pp. 140-146, 1977.
- Bell, A. T., "An Introduction to Plasma Etching [Semiconductor Device Fabrication]," Solid State Technology, Vol. 21, No. 4, pp. 89-94, 1978.
- Bersin, R. L., "A Survey of Plasma-Etching Process," Solid State Technology, Vol. 19, No. 5, pp. 31-36, 1976.
- Bersin, R. L., "Plasma Etching of Thin Metal and Dielectric Films," Journal of Vacuum Science and Technology, Vol. 13, No. 1, p. 169, 1976.

- Bersin, R. L., "Chemically Selective Anisotropic Plasma Etching," Solid State Technology, Vol. 21, No. 4, pp. 117-121, 1978.
- Bollinger, L. D., "Ion Milling for Semiconductor Production Process," Solid State Technology, Vol. 20, No. 11, pp. 66-70, 1977.
- Bondur, J. A., "Dry Process Technology (Reactive Ion Etching)," Journal of Vacuum Science and Technology, Vol. 13, No. 5, pp. 1023-1029, 1976.
- Brochu, M.; and Poulsen, R. G., "Importance of Temperature and Temperature Control in Plasma Etching," Electrochemical Society Spring Meeting, Washington, D. C., pp. 143-145, 1976.
- Chapman, B. N.; and Minkiewicz, V. J., "Flow Rate Effects in Plasma Etching," Journal of Vacuum Science and Technology, Vol. 15, No. 2, pp. 329-332, 1978.
- Clark, H. A., "Plasma Etching of SiO₂/Polysilicon Composite Film," IBM Technical Disclosure Bulletin, Vol. 20, No. 4, p. 1386, 1977.
- Clark, H. A., "Plasma Processing at Moderate Vacuum," Solid State Technology, Vol. 19, No. 6, pp. 51-54, 1976.
- Coburn, J. W.; Winters, H. F.; and Chuang, T. J., "Ion Surface Interaction in Plasma Etching," Journal of Applied Physics, Vol. 48, No. 8, pp. 3532-3540, 1977.
- Curran, J. E., "Vacuum Technology Applied to Electronic Component Fabrication," Journal of Vacuum Science and Technology, Vol. 14, No. 1, pp. 108-113, 1977.
- Devaney, J. R.; and Sheble, A. M., "Plasma Etching PROM and Other Problems," Solid State Technology, Vol. 17, No. 12, pp. 46-50, 1974.
- Dimigen, H.; and Luthje, H., "An Investigation of Ion Etching," Phillips Technology Review, Vol. 35, No. 7-8, pp. 199-208, 1975.
- Feeley, J. D.; and Alcorn, G. E., "Plasma Etching via Holes in Sputtered Quartz," IBM Technical Disclosure Bulletin, Vol. 17, No. 9, pp. 2701-2702, February 1975.
- Garceau, W. J., "Requirement for Compatibility Between Fluorine Plasma and Mounting Material in the Beam-Leaded Chip Separation Process," Electrochemical Society Fall Meeting, Las Vegas, Nevada, pp. 920-922, 1976.
- Garceau, W. J., "The Application of Fluorine Plasma Etch Process to the Chip Separation of Beam-Leaded Devices," Electrochemical Society Fall Meeting, Las Vegas, Nevada, pp. 923-925, 1976.

- Gloersen, P. G., "Masking for Ion Beam Etching," Solid State Technology, Vol. 19, No. 4, pp. 68-73, 1976.
- Gokan, H.; and Esho, E., "Fine Pattern Fabrication by Ion-Beam Etching," J. Vac. Soc. Japan (in Japanese), Vol. 20, No. 11, pp. 386-393, 1977.
- Griffiths, D. P.; and Bradley, S. H., "Plasma Etching as a Diagnostic Technique in Silicon Surface Studies," Journal of Material Science, Vol. 12, No. 5, pp. 1019-1027, 1977
- Hamamoto, M., "The Application of Gas Plasma for the Etching of Si_3N_4 Film and Its Effects on Photo-Resist," Electrochemical Society Fall Meeting, Dallas, Texas, p. 335, October 1975.
- Harris, D. H., "Are Plasma Sprayed Metallization on Microwave Ceramic Substrates," 12th Electrical/Electronics Insulation Conference, Boston, Massachusetts, pp. 99-101, November 1975.
- Harshbarger, W. R.; Porter, R. A.; Miller, T. A.; and Norton, P., "A Study of the Optical Emission from an RF Plasma During Semiconductor Etching," Applied Spectroscopy, Vol. 31, No. 3, pp. 201-207, 1977.
- Hawkins, D. T., "Ion Milling," Journal of Vacuum Science and Technology, Vol. 12, No. 6, pp. 1389-1398, 1976.
- Heinecke, R. A., "Plasma Reactor Design for the Selective Etching of SiO_2 on Si," Solid State Electronics, Vol. 19, No. 12, pp. 1039-1040, 1976.
- Heinecke, R. A. H., "Control of Relative Etch Rate of SiO_2 and Si in Plasma Etching," Solid State Electronics, Vol. 18, No. 12, pp. 1146-1147, December 1975.
- Heinecke, R. A. H., "Plasma Etching of Films at High Rates," Solid State Technology, Vol. 21, No. 4, pp. 104-106, 1978.
- Hollahan, J.; and Mitzel, J., "Application of Plasma to Semiconductor Materials and Fabrication," Proceedings of the Society of Photo-Optical Instrumentation Engineers, Vol. 55, pp. 110-115, August 1974.
- Horiike, Y.; and Shibagaki, M., "A New Chemical Dry Etching," Japanese Journal of Applied Physics, Vol. 15, Supplement 15-1, pp. 13-18, 1976.
- Jacob, A., "Application of Low Temperature RF Plasma Etching to Thin-Film Technology," Electrochemical Society Spring Meeting, Toronto, Canada, pp. 457-459, May 1975.

- Jacob, A., "The Versatile Technique of RF Plasma Etching. I. The Etch Profile," Solid State Technology, Vol. 19, No. 9, pp. 70-73, 1976.
- Jacob, A., "The Versatile Technique of RF Plasma Etching. II. Kinetics of Etchant Formation," Solid State Technology, Vol. 20, No. 6, pp. 31-36, June 1977.
- Jacob, A., "The Versatile Technique of RF Plasma Etching. III. Mechanistic Considerations for Selective Etching," Solid State Technology, Vol. 21, No. 4, pp. 95-98, 1978.
- Jacob, A., "Novel Selective RF Plasma Etching of Silicon and Silicon Containing Compounds Encountered in Semiconductor Manufacturer," Electrochemical Society Fall Meeting, Las Vegas, Nevada, pp. 917-919, 1976.
- Jinno, K.; Kinoshita, H.; and Matsuomoto, Y., "Etching Characteristics of Silicate Glass Films in CF₄ Plasma," Journal of Electrochemical Society, Vol. 124, No. 8, pp. 1258-1262, 1977.
- Jinno, K.; Kinoshita, H.; and Matsuomoto, Y., "Etching Characteristics of Silicate Glasses in CF₄ Plasma Etching," Electrochemical Society Fall Meeting, Las Vegas, Nevada, pp. 751-753, October 1976.
- Kinoshita, H.; and Jinno, K., "Anisotropic Etching of Silicon by Gas Plasma," Japanese Journal of Applied Physics, Vol. 16, No. 2, pp. 381-382, 1977.
- Kinoshita, T., "Plasma Electron Beam Source and Its Application to Vacuum Metallurgy," J. Vac. Soc. Japan, Vol. 17, No. 12, pp. 423-437, 1974.
- Kirk, R. W., "Application of Plasma Technology to the Fabrication of Semiconductor Devices," Techniques and Applications of Plasma Etching, J. R. Hollohan (Ed.), 1974.
- Komiya, H.; Abe, H.; Sonobe, Y.; and Matsui, H., "The Application of Gas Plasma to the Fabrication of MOS-LSI," 1973 International Electron Device Meeting Technical Digest, pp. 459-462.
- Komiya, H.; Toyoda, H.; Kato, T.; and Inaba, K., "Microfabrication Technique by Gas Plasma Etching Method," Japanese Journal of Applied Physics, Vol. 15, Supplement 15-1, pp. 19-24, 1976.
- Kumar, R.; and Ladas, C., "Characterization of Plasma-Etching for Semiconductor Application," 1975 International Electron Devices Meeting, pp. 27-28.
- Kumar, R.; Ladas, C.; and Hudson, G., "Characterization of Plasma Etching for Semiconductor Applications," Solid State Technology, Vol. 19, No. 10, pp. 54-59, 1976.

- Laznovsky, W., "Advances in Low Energy Ion Beam Technology," Research/Development, Vol. 26, No. 8, pp. 47-55, August 1975.
- Legat, W. H.; and Schilling, H., "Plasma Etching of Metal Films in the Fabrication of Large Scale Integrated Circuits," Electrochemical Society Fall Meeting, Dallas, Texas, pp. 336-338, October 1975.
- Lehman, H. W.; and Widmer, R., "Profile Control by Reactive Sputter Etching," Journal of Vacuum Science and Technology, Vol. 15, No. 2, pp. 319-326, 1978.
- Mader, L.; and Hoepfner, J., "Ion Beam Etching of Silicon Dioxide on Silicon," Journal of the Electrochemical Society, Vol. 123, No. 12, pp. 1893-1898, 1976.
- Mader, L.; Widmann, D.; and Hopfner, J., "Ion Beam Etching of Silicon Dioxide Layers for MOS Devices," Electrochemical Society Spring Meeting, Toronto, Canada, pp. 432-433, May 1975.
- Maeda, K.; and Fujino, K., "Patterning of Metal Films by Gas Plasma Technique," Denki Kagaku, Vol. 43, pp. 22-27, 1975.
- Maddox, R. L.; and Parker, H. L., "Application of Reactive Plasma Practical Microelectronic Processing Systems," Solid State Technology, Vol. 21, No. 4, pp. 107-113, 1978.
- Matsuo, S.; and Takehara, Y., "Preferential SiO_2 Etching on Si Substrate by Plasma Reactive Sputter Etching," Japanese Journal of Applied Physics, Vol. 16, No. 1, pp. 175-176, 1977.
- Matsuo, S.; Takamoto, K.; and Nakayama, S., "Pattern Formation Process by Ion Etching," J. Jap. Soc. Precis. Eng. (Japan), Vol. 42, No. 6, pp. 493-500, June 1976.
- Matsuo, S., "Etching Characteristics of Various Materials by Plasma Reactive Sputtering Etching," Japanese Journal of Applied Physics, Vol. 17, No. 1, pp. 235-236, 1978.
- Melliar-Smith, C. M., "Ion Etching for Pattern Delineation," Journal of Vacuum Science and Technology, Vol. 13, No. 5, pp. 1000-1022, 1976.
- Mimura, Y., "Fine Pattern Fabrication Using Freon Gas Plasma Etching," J. Jap. Soc. Precis. Eng. (Japan), Vol. 42, No. 6, pp. 485-492, June 1976.
- Mogab, C. J.; and Shankoff, T. A., "Plasma Etching of Titanium for Application to the Patterning of Ti-Pd-Au Metallization," Journal of the Electrochemical Society, Vol. 124, No. 11, pp. 1766-1771, 1977.

- Mogab, C. J., "The Loading Effect in Plasma Etching," Journal of the Electrochemical Society, Vol. 124, No. 8, pp. 1262-1268, 1977.
- Magab, C. J.; Adams, A. C.; and Flamm, D. L., "Plasma Etching of Si and SiO₂--The Effect of Oxygen Additions to CF₄ Plasma," Journal of Vacuum Science and Technology, Vol. 15, No. 2, p. 333, 1978.
- Poulsen, R. G.; Nentwich, H.; and Ingrey S., "Plasma Etching of Aluminum," 1976 International Electron Device Meeting Technical Digest, pp. 205-208.
- Poulsen, R. G., "Plasma Etching in Integrated Circuit Manufacture--A Review," Journal of Vacuum Science and Technology, Vol. 14, No. 1, pp. 266-274, 1977.
- Poulsen, B., "Plasma Etching--A New Technique for Integrated Circuit Fabrication," Telesis (Canada), Vol. 5, No. 3, pp. 73-79, 1977.
- Reinberg, A. R., "Plasma Etching in Semiconductor Manufacture--An Overview," Electrochemical Society Spring Meeting, Washington, D. C., p. 142, May 1976.
- Rodriguez, A.; Misra, M.; Hesselbom, H.; and Tove, P. A., "Fabrication of Short Channel MOSFET with Refractory Metal Gates Using RF Sputtering Etching," Solid State Electronics, Vol. 19, No. 1, pp. 17-21, January 1976.
- Schaible, P. M.; Metzger, W. C.; and Anderson, J. P., "Reactive Ion Etching of Aluminum and Aluminum Alloys in an RF Plasma Containing Halogen Species," Journal of Vacuum Science and Technology, Vol. 15, No. 2, pp. 334-337, 1978.
- Schwartz, G. C.; Zielinski, L.; and Schopen, T., "Reactive Ion Etching; Frequency and Loading Effects," Electrochemical Society Spring Meeting, Washington, D. C., p. 146, May 1976.
- Sheble, A. M.; Teel, T. P.; and Devaney, J. R., "Plasma Etching for SEM and EMP Examination of Microelectronic Devices," 9th Annual Conference of the Microbeam Analysis Society, Ottawa, Canada, 31A/App, July 1974.
- Sinka, A. K.; Levinstein, H. L.; Smith, T. E.; Quintana, G.; Haszko, S. E., "Reactive Plasma Deposited Si₃N₄ Films for MOS-LSI Passivation," Journal of the Electrochemical Society, Vol. 125, No. 4, pp. 601-608, 1978.
- Smith, H. I., "Ion Beam Etching," Electrochemical Society Spring Meeting, Washington, D. C., p. 148, May 1976.

- Somekh, S., "Introduction to Ion and Plasma Etching," Journal of Vacuum Science and Technology, Vol. 13, No. 5, pp. 1003-1007, 1976.
- Somekh, S.; Casey, H. C., Jr.; and Ilegems, M., "Preparation of High-Aspect Ratio Periodic Corrugations by Plasma and Ion Etching," Applied Optics, Vol. 15, No. 8, pp. 1905-1906, August 1976.
- Spencer, E. G., Lenzo, P. V.; and Schmidt, P. H., "Ion-Etching of Thin Windows in Silicon," Journal of Vacuum Science and Technology, Vol. 11, No. 5, pp. 863-864, 1974.
- Stafford, W. B.; and Gorin, G. J., "Optical Emission End-Point Detecting for Monitoring Oxygen Plasma Photoresist Stripping," Solid State Technology, Vol. 20, No. 9, pp. 51-55, 1977.
- Suzuki, K.; Okadaira, S.; Sakudo, N.; and Kanomata, I., "Microwave Plasma Etching," Japanese Journal of Applied Physics, Vol. 16, No. 11, pp. 1979-1984, 1977.
- Ukai, K.; and Hanazawa, K., "Analysis of the Imaging Accuracy in Reactive Ion Etching," Journal of Vacuum Science and Technology, Vol. 15, No. 2, pp. 338-340, 1978.
- Voshchenkov, A. M., "Shielded Plasma Etching of Polysilicon--MOS Structure: A C-V Evaluation," Electrochemical Society Fall Meeting, Dallas, Texas, pp. 333-334, October 1975.
- Winters, H. F.; and Coburn, J. W., "Plasma Etching--A Pseudo Black Box Approach," Journal of Applied Physics, Vol. 48, No. 12, pp. 4973-4983, 1977.
- Zafiropulo, A., "Dry vs. Wet-Plasma Etching/Stripping Comes of Age," Circuit Manufacturing, Vol. 16, No. 4, pp. 42, 44, 46, April 1976.
- Zielinski, L.; and Schwartz, G. C., "Reactive Ion Etching," Electrochemical Society Spring Meeting, Toronto, Canada, pp. 117-118, May 1975.

APPENDIX D

PROGRAM NOTATION

A = AG	K7 = K ₂₁
B = B	K8 = K ₂₂
B1 = B1	K9 = K ₂₃
B2 = B1 _{mn}	L = TL
B3 = B1 _{mx}	M = MU
C1 = \$W	N = N
C2 = \$AC	N1 = n
C3 = \$TC	N2 = n _r
C5 = \$RPL	N3 = N _m
C6 = \$RPR	N4 = NA
C7 = \$CB	N9 = NC
C8 = \$TG	F = BP
C9 = K _c	R1 = \$CE
D = D _n	R2 = \$CAD
D1 = d	R3 = \$ML
F = f	S = NES
G = NG	S1 = NESS
K1 = K ₁	T = β ₀
K3 = K ₃	Y3 = Y _A
K4 = K _p	Y4 = Y _{FT}
K5 = K _A	

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08:29 JUN 04, '79 JD=0AFD
JOB G00L0,FC45020(NAST/CAD),1
LIMIT (TIME,20), (CORE,25)
BASIC
VER, D03
BASIC
WIDTH= 72 PRG= 6
$= 72
LOAD COOKS2
WID 132
SFT 3=132
LIST
3 DATA 10,20,50,100,200,500,1E3,1F4,1E5,1E6
5 USING 31
6 READ 3
10 FOR G1=1 TO 4 STEP .2
20 GOSUB 100
25 GOSUB 2000
31 TYPE GATE SK TOT: CHIP INDES MASH PART REPL REPR ICM: CFAB CIRU CADL MANL RETI CASH CIST
33 USING 33, 'F-C', G, N3, C8, V1, V2, V3, V4, V5, V6, X, X1, X2, X3, X4, X5, X6, X7
34 USING 33, 'F-C', G, N3, C8, V1, V2, V3, V4, V5, V6, X, X1, X2, X3, X4, X5, X6, X7
35 GOSUB 3000
37 GOTO 70
40 GOSUB 200
45 GOSUB 2000
55 USING 33, 'S-C', G, N3, C8, V1, V2, V3, V4, V5, V6, X, X1, X2, X3, X4, X5, X6, X7
70 USING 33, 'STD', G, N3, C8, V1, V2, V3, V4, V5, V6, X, X1, X2, X3, X4, X5, X6, X7
80 GOSUB 2000
85 USING 33, 'D-M', G, N3, C8, V1, V2, V3, V4, V5, V6, X, X1, X2, X3, X4, X5, X6, X7
90 NEXT G1
95 PAGE
96 GOTO 5
100 A=.025 & D1=1.00 & D=.0155 & C1=200 & Y3=.95 & Y4=.90 & P=.0375
110 K4=3 & H1=15 & K1=1 & R2=220 & K3=1 & R3=10 & T=3
111 R1=A/K4
115 K7=1.0E-2 & K8=7E-4 & K9=1.0E-2
120 R2=H1/2 & R3=4*B2 & C2=.1*K4*G**5 & C3=.2*K4*G**5
150 B=.05 & L=.05000 & M=2 & F=6 & N=10000
160 C7=50 & N2=7 & N1=6
161 K5=.8
162 Y3=.95 & Y4=.9
163 S1=S*SQR(N/G)
165 C5=200+2*K4*H**5*(1+(S/S1)**.5)
150 N4=1
150 N4=1
199 RETURN
200 A=.1 & B1=2*A/K4 & R2=B1/2 & R3=4*B2 & F=1 & N2=1 & K5=.4 & N1=6
209 RETURN
400 R2=3 & N1=6 & F=3

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410 RETURN
1000 N3=H4*S*(1+B*(S/S1))*L*(N/G)*2.5E-6*LG(T(G))
1001 N3=NUMBER MANUFACTURED OF ONE TYPE IC
1100 F9=A*G+H1*K4*G+P*K4*G**5
1101 C4=C1*(4/(5.14*01)*2*Y3*Y4))*F9*(1+D*K5*F9)**N1
1102 X1=C4/G
1107 X1=IC FAN COST PER GATE
1110 CIR DFS COST PER GATE=X2
1112 X2=H1*K1*K4*(1-1/G**5)/N3
1120 CAD COST PER GATE=X3
1122 X3=H2*(LOG(G)*(K7+K8*K4)+K9*N2)*K4/N3
1130 MAN LAYOUT OPTIM. COST PER GATE=X4
1131 X4=H3*F*(K4/(1*N3))*LOG((H3-H2)/(H1-H2))
1140 RETICLE COST PER GATE=X5
1142 X5=H5*N2*K4/N3
1150 ASSEMBLY COST PER GATE=X6
1152 X6=C2/(Y3*Y4*G)
1160 TEST COST PER GATE=X7
1162 X7=C3/(Y4*G)
1170 MANUF. COST PER IC=X4*X6
1171 X=X1+X2+X3+X4+X5+X6+X7
1172 C4=X*G
1200 TOTAL COST PER GATE($1G)=C4=CHIPS*MOD:DES+MOD:ASSY+PARTS+REPLACE+REPAIR
1210 EFFECTIVE GATE FAILURE RATE=Z
1211 Z=2.5E-6*LG(T(G))/G
1220 CHIPS
1221 V1=(1+B*S*L*N*Z/S1)*C4*M/G
1230 MOD:DES
1231 C9=K4*G**5
1232 N9=N*S/(G*S1)
1233 V2=(N*C9/(G*N3))*H1*K1*(1-1/N9**5)+P2*(LOG(N9)*(K7+K8*C9)+3*K9)+3*K3)
1234 V2=V2+2*H3*C9*H*LOG(3)/(1*N3*G)
1235 V2=V2/N
1240 MOD:ASSY=V3
1241 V3=(2*C9*750+5000/H3+10*C9*(N9*S1/S)**5)*S1/(S*N)
1250 PART9=V4
1251 V4=(1-B)*C7*L*Z
1260 REFLACE=V5
1261 V5=L*Z*H*C5
1262 C6=C5*(V2+V3)*N*S/(S1*10)
1270 REPAIR=V6
1271 V6=L*Z*(1-B)*C6
1280 C8=V1+V2+V3+V4+V5+V6
1999 RETURN
2000 I=1 & T8=0
2010 FOR I=1 TO 10
2020 T8=T8+I*2*(10-I)
2030 H1=H2*(H3-H2)*.99**T8 & GOSUB 1000
2040 M8=CR
2050 B1=H2*(H3-H2)*.99**T8+1 & GOSUB 1000
2060 IF CR<M8 THEN 2080
2070 I=-1
```

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2080 NEXT T9
2100 RETURN
3000 N3=I*6 & I=1 & TR=0
3002 FOR T9=1 TO 10
3004 TR=TR+I*2** (10-T9)
3005 N1=H2+(H3-H2)*.99**TR & GOSUB 1001
3006 M4=C4
3010 B1=H2+(H3-H2)*.99** (TR+1) & GOSUB 1001
3020 IF C4<M4 THEN 3040
3030 I=-1
3040 NEXT T9
3100 F1=X1 & F2=X2 & F3=X3 & F4=X4 & F5=X5 & F6=X6 & F7=X7 & F8=X
3102 GOSUB 1000
3104 X1=F1 & X2=F2 & X3=F3 & X4=F4 & X5=F5 & X6=F6 & X7=F7 & X=F8
3110 C4=X*GRV1=(1+R*S*L*N*2/S1)*C4*M/GR*CR=V1+V2+V3+V4+V5+V6
3120 RETURN
FAST

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